DESCRIPTION

These monolithic dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

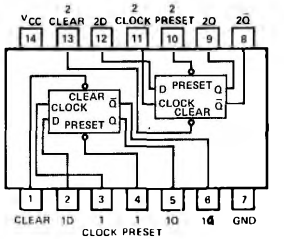
Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10-normalized series 54S/74S loads is available from each of the outputs at low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 75 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The N74S74 is characterized for operation from 0°C to 70°C.

Typical Maximum Input Clock Frequency	90 MHz
Typical Power Dissipation	75 mW per Flip-Flop

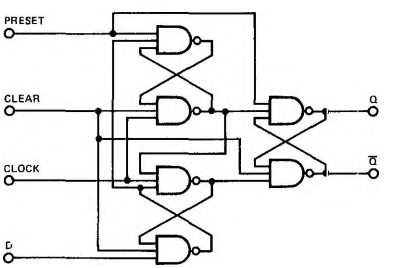
PIN CONFIGURATION



Positive Logic:

Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

FUNCTIONAL BLOCK DIAGRAM (EACH FLIP-FLOP)



TRUTH TABLE (Each Flip-Flop)

t_n	$t_n + 1$	
INPUT	OUTPUT	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = High level, L = Low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Clock frequency, f_{clock}			70		MHz
Width of clock pulse, t_w (clock)			7		ns
Width of preset pulse, t_w (preset)			7		ns
Width of clear pulse, t_w (clear)			7		ns
Input set-up time, t_{setup}	High level data		10		ns
	Low level data		12		
Input hold time, t_{hold}		0			ns
Operating free-air temperature, T_A		0		70	°C

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High level input voltage			2			V
V_{IL}	Low level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High level output voltage	V_{CC} = MIN,	V_{IH} = 2 V	2.7	3.4		V
		V_{IL} = 0.8,	I_{OL} = 20 mA				
V_{OL}	Low level output voltage	V_{CC} = MIN,	V_{IH} = 2 V			0.5	V
		V_{IL} = 0.8,	I_{OL} = 20 mA				
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High level input current	V_{CC} = MAX,	D input			50	μA
		V_I = 2.7 V	Clock or Preset			100	
			Clear			150	
I_{IL}	Low level input current	V_{CC} = MAX,	D input			−2	mA
		V_I = 0.5 V	Clock or Preset			−4	
			Clear			−6	
I_{OS}	Short circuit output current‡	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = MAX,	See Note 1		30		mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω NOTE 1		90		MHz
t_{PLH}	Propagation delay time, low-to-high level output, from clear or preset			5		ns
t_{PHL}	Propagation delay time, high-to-low level output, from clear or preset			8		ns
t_{PLH}	Propagation delay time, low-to-high level output, from clock			7		ns
t_{PHL}	Propagation delay time, high-to-low level output, from clock			7		ns

NOTE 1: Load circuit and test waveforms are shown on page 2-293