DESCRIPTION

The 54/74S200/201 and 54/74S301 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors, which reduces input loading to 25μA for a high level and -250μA (S54S200/201/301) or -100μA (N74S200/201/301) for a low level.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H" or "Hi-Z" state) permits $\overline{D}_O$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast read access and write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

They are available in both the commercial and military temperature ranges. The commercial temperature range (0°C to +75°C) is specified as N74S200/201/301, F or N, and the military temperature range (-55°C to +125°C) is specified as S54S200/201/301, F only.

FEATURES

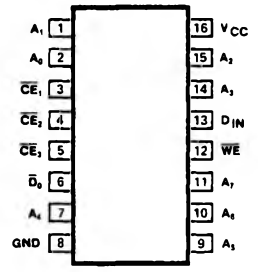
- **Address access time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 70ns max
- **Write cycle time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 60ns max
- **Power dissipation : 1.5mW/bit typ**
- **Input loading:**
  N74S200/201/301: -100μA max
  S54S200/201/301: -250μA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Output option:**
  54/74S200/201: Tri-state
  54/74S301: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

F,N PACKAGE*



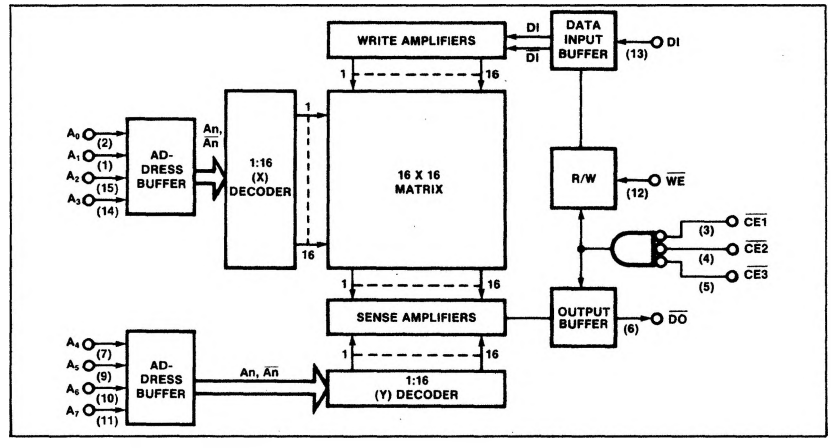
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				54/74S301	54/74S200/201
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (54/74S301)	+5.5	
V_O	Off-state (54/74S200/201)	+5.5	
	Temperature range		°C
T_A	Operating		
	N74S200/201/301	0 to +70	
	S54S200/201/301	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N74S200/201/301			S54S200/201/301			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low[2]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[2]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp [2,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[2,4]	I_{OL} = 16mA		0.35	0.45		0.30	0.50	
V_{OH}	High (N74S200/201)[2,5]	I_{OH} = 10.3mA	2.4						
V_{OH}	High (S54200/201)[2,5]	I_{OH} = -5.2mA				2.4			
	Input current[3]	V_{CC} = Max							
I_I	At V_{IN} Max	V_{IN} = 5.5V			1			1	mA
I_{IL}	Low	V_{IL} = 0.45V		-10	-100		-10	-250	μA
I_{IH}	High	V_{IH} = 2.7V		1	25		1	25	μA
	Output current								
I_{OLK}	Leakage (54/74S301)[6]	V_{IH} = 2V, V_O = 5.5V		1	40		1	50	μA
$I_{O(OFF)}$	Hi-Z state (54/74S200/201)[6]	V_{CC} = Max, V_O = 5.5V		1	40		1	100	μA
		V_{IH} = 2V, V_O = 0.4V		-1	-40		-1	-100	
I_{OS}	Short circuit (54/74S200/201)[7]	V_{CC} = Max, V_O = 0V	-30		-100	-30		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC}= Max		80	130		80	130	mA
		V_{CC} = Max, T_A = +125°C						99	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R_L = 270Ω, C_L = 15pF, See ac test load

N74S200/201/301: 0°C ≤ T_A ≤ +70°C, 4.75V ≤ V_{CC} ≤ 5.25V

S54S200/201/301: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S200/201			S54S200/201			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address			40	50		40	70	
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	R_{L1}=270Ω, R_{L2}=1kΩ							
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable				35			45	
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	R_{L1}=270Ω, R_{L2}=1kΩ							
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	C_L=5pF			20			30	
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable	R_{L1}=270Ω, R_{L2}=1kΩ							
t_{PHL}	High to low [C,D,E]		Write enable								
t_{LZ}	Low [D,G]	Output	Write enable	C_L=5pF			30			40	
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]						40			50	
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]										
	Pulse width [H]										ns
t_W	Write enable			R_{L1}=270Ω, R_{L2}=1kΩ	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address		0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Address	R_{L1}=270Ω, R_{L2}=1kΩ							
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Data		40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Data	R_{L1}=270Ω, R_{L2}=1kΩ							
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Chip enable		0			0			
t_H	Hold time	Chip enable	Write enable		0			0			
t_S	Setup time	Write enable	Chip enable	R_{L1}=270Ω, R_{L2}= 1kΩ							
t_H	Hold time	Chip enable	Write enable								

AC ELECTRICAL CHARACTERISTICS

(Cont'd) $R_L = 270\Omega$, $C_L = 15pF$, See ac test load
N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$
S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

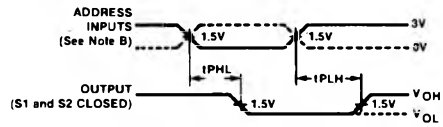
PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S301			S54S301			UNIT
					Min	Typ[1]	Max	Min	Typ	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address								
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$		40	50		40	70	
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable								
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			35			45	
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	$C_L=5pF$							
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			20			30	
t_{PHL}	High to low [C,D,E]		Write enable				30			40	
t_{LZ}	Low [D,G]	Output	Write enable	$C_L=5pF$							
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]										
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]						40			50	
	Pulse width [H]										ns
t_W	Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address								
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Data								
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Chip enable								
t_H	Hold time	Chip enable	Write enable								
t_S	Setup time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Chip enable	Write enable		0			0			

NOTES

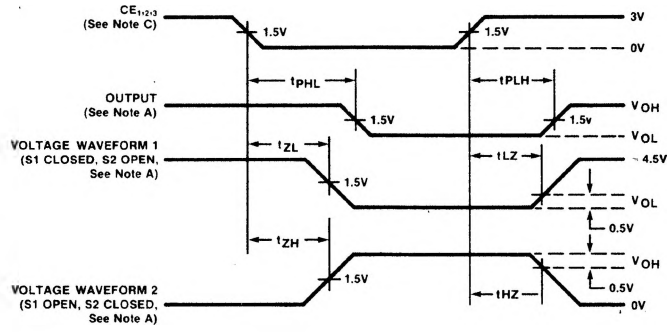
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with logic stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. See timing diagram notes.

TIMING DIAGRAMS

READ CYCLE

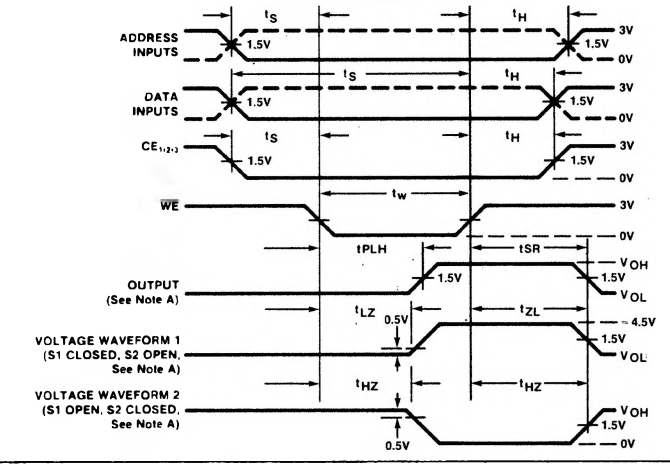


Address Time From Address



Chip Enable and Disable Time

WRITE CYCLE

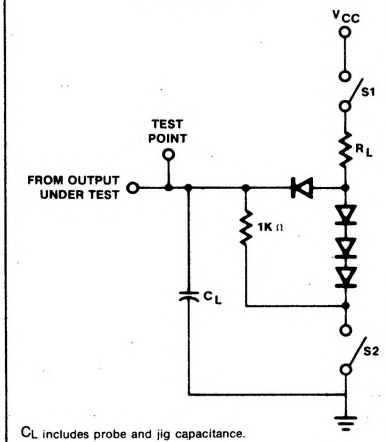


NOTES

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR $\leq$ 1MHz, and $Z_{OUT} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low level output.
F. t_{ZH} propagation delay time, Hi-Z to high level output, t_{ZL} propagation delay time, Hi-Z to low level output.
G. T_{HZ} propagation delay time, high level to Hi-Z output, t_{LZ} propagation delay time, low level to Hi-Z output.
H. Minimum required to guarantee a Write into the slowest bit.

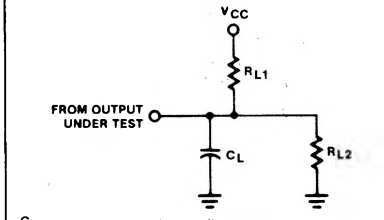
TEST LOAD CIRCUITS

54/74S200/201



C_L includes probe and jig capacitance.
All diodes are 1N3064.

54/74S301



C_L includes probe and jig capacitance.
All diodes are 1N3064.