

54/74125 54LS/74LS125A

QUAD BUS BUFFER GATE

(With 3-State Outputs)

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74125PC, 74LS125APC		9A
Ceramic DIP (D)	A	74125DC, 74LS125ADC	54125DM, 54LS125ADM	6A
Flatpak (F)	A	74125FC, 74LS125AFC	54125FM, 54LS125AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

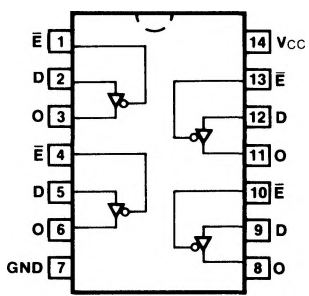
PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
V _{OH}	Output HIGH Voltage	XM	2.4			V	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}
		XC	2.4				
		XM		2.4			
		XC		2.4			
I _{OS}	Output Short Circuit Current	XM	-30 -70	-30 -130		mA	V _{CC} = Max
		XC	-28 -70	-30 -130			
I _{CC}	Power Supply Current		54	20		mA	Outputs OFF, V _{IN} = Gnd V _E = 4.5 V, V _{CC} = Max
t _{PLH}	Propagation Delay Data to Output		13	15		ns	Figs. 3-3, 3-5
t _{PHL}			18	18			
t _{PZH}	Output Enable Time		17	16		ns	Figs. 3-3, 3-11, 3-12
t _{PZL}			25	25			
t _{PLZ}	Output Disable Time		8.0	25		ns	Figs. 3-3, 3-11, 3-12
t _{PHZ}			12	25			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

CONNECTION DIAGRAM PINOUT A



TRUTH TABLE

INPUTS		OUTPUT
E-bar	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance