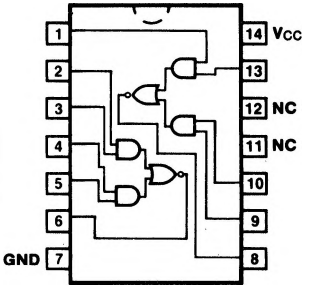
54/7451
54H/74H51
54S/74S51
54LS/74LS51

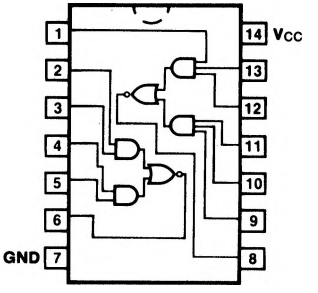
DUAL 2-WIDE, 2-INPUT AOI GATE
DUAL 2-WIDE, 2-INPUT/3-INPUT AOI GATE ('LS51)

CONNECTION DIAGRAMS

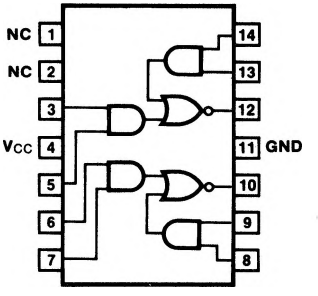
PINOUT A



PINOUT B



PINOUT C



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7451PC, 74H51PC 74S51PC		9A
	B	74LS51PC		
Ceramic DIP (D)	A	7451DC, 74H51DC 74S51DC	5451DM, 54H51DM 54S51DM	6A
	B	74LS51DC	54LS51DM	
Flatpak (F)	A	74S51FC	54S51FM	3I
	B	74LS51FC	54LS51FM	
	C	7451FC, 74H51FC	5451FM, 54H51FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply		8.0		12.8		17.8		1.6	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}	Current		14		24		22		2.8		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay		22		11	2.0	5.5		20	ns	Figs. 3-1, 3-4
t_{PHL}			15		11	2.0	5.5		20		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.