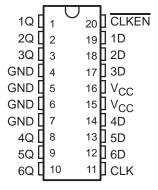
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- Inputs Are TTL-Voltage Compatible
- Contains Six D-Type Flip-Flops
- Clock Enable Latched to Avoid False Clocking
- Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC ™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

DW OR N PACKAGE (TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a clock-enable input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock-enable input (CLKEN) is low.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock inputs are at either the high or low level, the data (D) input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the clock-enable (CLKEN) input.

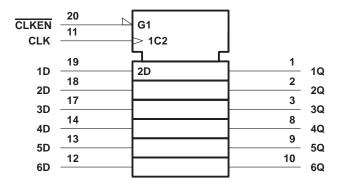
The 74ACT11378 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE (each flip-flop)

IN	IPUTS	OUTPUT	
CLKEN	CLK	D	Q
Н	Χ	Х	QO
L	\uparrow	Н	Н
L	\uparrow	L	L
Х	L	Χ	QO

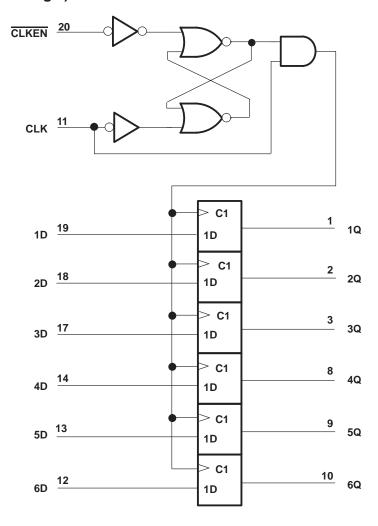
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±150 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V_{IL}	Low-level input voltage			8.0	V
VI	Input voltage	0		VCC	V
VO	Output voltage	0		VCC	V
IOH	High-level output current			-24	mA
lOL	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	ns/V
TA	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	.,	T _A = 25°C					
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	UNIT
		4.5 V	4.4			4.4		
	$I_{OH} = -50 \mu\text{A}$	5.5 V	5.4			5.4		1
∨он	044	4.5 V	3.94			3.8		V
	$I_{OH} = -24 \text{ mA}$	5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{\ddagger}$	5.5 V				3.85		
	I _{OL} = 50 μA I _{OL} = 24 mA	4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
VoL		4.5 V			0.36		0.44	V
		5.5 V			0.36		0.44	
	I _{OL} = 75 mA [‡]	5.5 V					1.65	
lį	V _I = V _{CC} or GND	5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μΑ
ΔICC§	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1	mA
C _i	V _I = V _{CC} or GND	5 V		4.5				pF

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

74ACT11378 HEX D-TYPE FLIP-FLOP WITH CLOCK ENABLE

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timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			T _A =	25°C			
			MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency		0	100	0	100	MHz
t _W	Pulse duration	CLK high or low	5		5		ns
	0	Data	5		5		
tsu	Setup time, before CLK↑	CLKEN high or low	4.5		4.5		ns
		Data	0.5		0.5		
^t h	Hold time, after CLK↑ CLKEN high		1		1		ns

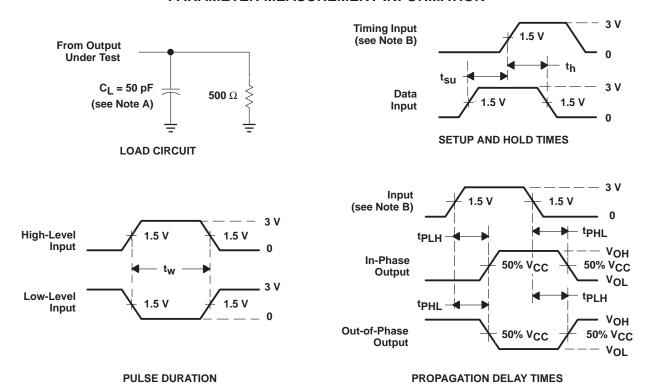
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T,	4 = 25°C	;			
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
f _{max}			100	130		100		MHz
t _{PLH}	011/	A O	2.8	5.9	6.8	2.8	9	
^t PHL	CLK	Any Q	3.7	7.3	9.2	3.7	10.7	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS TYP		UNIT
C _{pd}	Power dissipation capacitance	$C_I = 50 \text{ pF}, \qquad f = 1 \text{ MHz}$	31	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns. For testing t_{max} and pulse duration: $t_r = 1$ to 3 ns, $t_f = 1$ to 3 ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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