# 54/7470

## JK EDGE-TRIGGERED FLIP-FLOP

**DESCRIPTION** — The '70 is a gated input edge-triggered JK flip-flop offering Direct Clear and Set inputs, and complementary Q and $\overline{Q}$ outputs. Information at the J and K inputs is tranferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specified voltage level of the clock pulse. When the clock input threshold voltage has been passed, the gate inputs are locked out. These flip-flops are designed for medium to high speed applications and offer a significant saving in system power dissipation and package count where input gating is required.

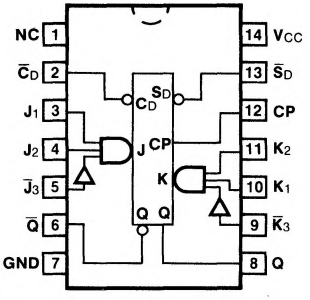
**TRUTH TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| @ $t_n$ | | @ $t_{n+1}$ |
| J | K | Q |
| L | L | $Q_n$ |
| L | H | L |
| H | L | H |
| H | H | $\overline{Q}_n$ |

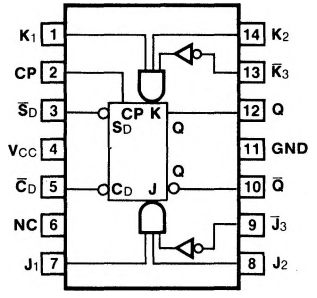
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear or Set function can only occur when clock input is LOW
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is indeterminate

$J = J_1 \bullet J_2 \bullet \overline{J}_3$
$K = K_1 \bullet K_2 \bullet \overline{K}_3$
$t_n$ = Bit time before clock pulse.
$t_{n+1}$ = Bit time after clock pulse.
If inputs $\overline{J}_3$ or $\overline{K}_3$ are not used they must be grounded.
H = HIGH Voltage Level
L = LOW Voltage Level

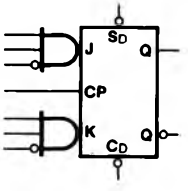
**CONNECTION DIAGRAMS**
PINOUT A




PINOUT B




**LOGIC SYMBOL**




$V_{CC}$ = Pin 14 (4)
GND = Pin 7 (11)

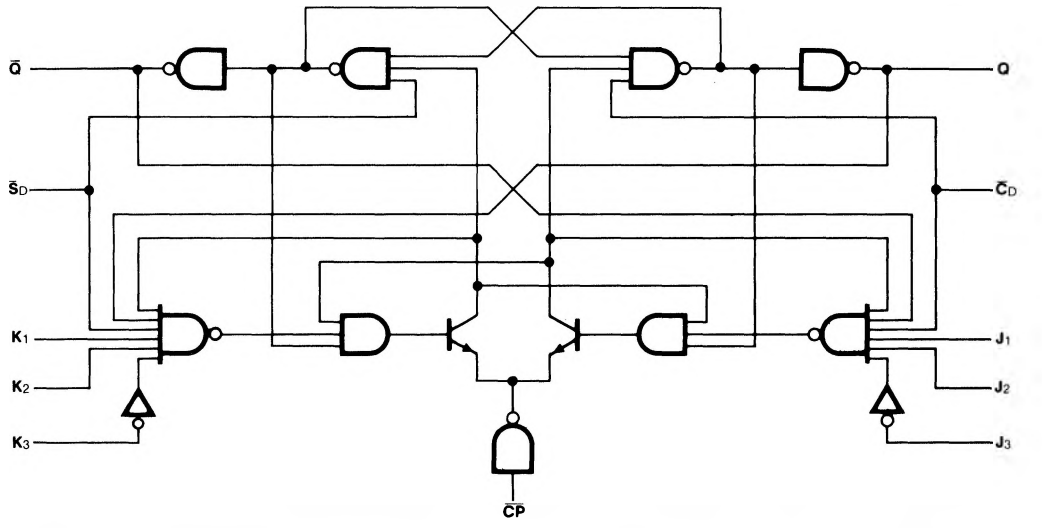
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>$V_{CC}$ = +5.0 V ±5%,<br>$T_A$ = 0°C to +70°C | MILITARY GRADE<br>$V_{CC}$ = +5.0 V ±10%,<br>$T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7470PC | | 9A |
| Ceramic DIP (D) | A | 7470DC | 5470DM | 6A |
| Flatpak (F) | B | 7470FC | 5470FM | 3I |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74 (U.L.) HIGH/LOW |
|---|---|---|
| $J_1$, $J_2$, $\overline{J}_3$<br>$K_1$, $K_2$, $\overline{K}_3$ | Data Inputs | 1.0/1.0 |
| CP | Clock Pulse Input (Active Rising Edge) | 1.0/1.0 |
| $\overline{C}_D$ | Direct Clear Input (Active LOW) | 2.0/2.0 |
| $\overline{S}_D$ | Direct Set Input (Active LOW) | 2.0/2.0 |
| Q, $\overline{Q}$ | Outputs | 20/10 |

## LOGIC DIAGRAM




**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74 | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $I_{CC}$ | Power Supply Current | | 26 | mA | $V_{CC}$ = Max, $V_{CP}$ = 0 V |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | DESCRIPTION | 54/74 $C_L$ = 15 pF, $R_L$ = 400 Ω | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 20 | | MHz | Fig. 3-1, 3-8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to Q or $\overline{Q}$ | | 50<br>50 | ns | Figs. 3-1, 3-8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{S}_D$ or $\overline{C}_D$ to Q or $\overline{Q}$ | | 50<br>50 | ns | Figs. 3-1, 3-10 |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C

| SYMBOL | PARAMETER | 54/74 | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_s$ (H) | Setup Time HIGH, $J_n$ or $K_n$ to CP | 20 | | ns | Fig. 3-6 |
| $t_h$ (H) | Hold Time HIGH, $J_n$ or $K_n$ to CP | 5.0 | | ns | Fig. 3-6 |
| $t_s$ (L) | Setup Time LOW, $J_n$ or $K_n$ to CP | 20 | | ns | Fig. 3-6 |
| $t_h$ (L) | Hold Time LOW, $J_n$ or $K_n$ to CP | 5.0 | | ns | Fig. 3-6 |
| $t_w$ (H)<br>$t_w$ (L) | CP Pulse Width | 20<br>30 | | ns | Fig. 3-8 |
| $t_w$ (L) | $\overline{S}_D$ or $\overline{C}_D$ Pulse Width LOW | 25 | | ns | Fig. 3-10 |