DESCRIPTION

The NE562B Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system, comprising a VCO, phase comparator, amplifier and low pass filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by two capacitors and two resistors at the phase comparator output.

This PLL has two sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division applications. Terminals are also provided for the optional extension of the tracking range. The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%

FEATURES

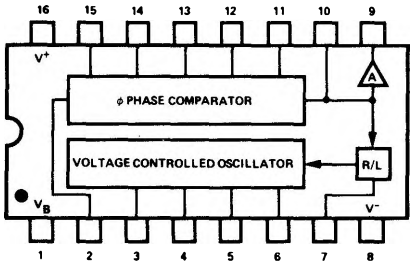
- **FREQUENCY MULTIPLICATION AND DIVISION**
- **SIGNAL CONDITIONING AND SIDE-BAND SUPPRESSION**
- **FM DEMODULATION WITHOUT TUNED CIRCUITS**
- **NARROW BANDPASS – TO ±1%**
- **ADJUSTABLE TRACKING RANGE – TO ±15%**
- **EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT**
- **HIGH LINEARITY – 1% DISTORTION MAXIMUM AT 1% DEVIATION**

APPLICATIONS

FREQUENCY SYNTHESIZERS
DATA SYNCHRONIZERS
SIGNAL CONDITIONING
TRACKING FILTERS
TELEMETRY DECODERS
MODEMS
FM IF STRIPS AND DEMODULATORS
TONE DECODERS
FSK RECEIVERS
WIDEBAND HIGH LINEARITY FM DEMODULATORS

PIN CONFIGURATION

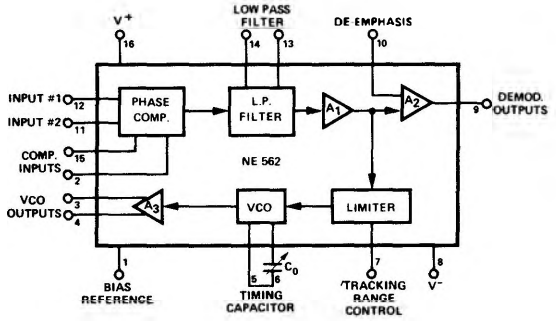
B PACKAGE
(Top View)



1. Bias Reference Voltage
2. Phase Comparator Input #1
3. VCO Output #1
4. VCO Output #2.
5. VCO Timing Capacitor
6. VCO Timing Capacitor
7. Range Control
8. Negative Power Supply (Ground)
9. Demodulated FM Output (an open emitter)
10. De-emphasis (Audio Bandshaping)
11. RF Input #1
12. RF Input #2
13. Low-Pass Loop Filter
14. Low-Pass Loop Filter
15. Phase Comparator Input #2
16. Positive Power Supply

ORDER PART NO. NE562B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Maximum Operating Voltage	30V
Input Voltage	3V rms
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

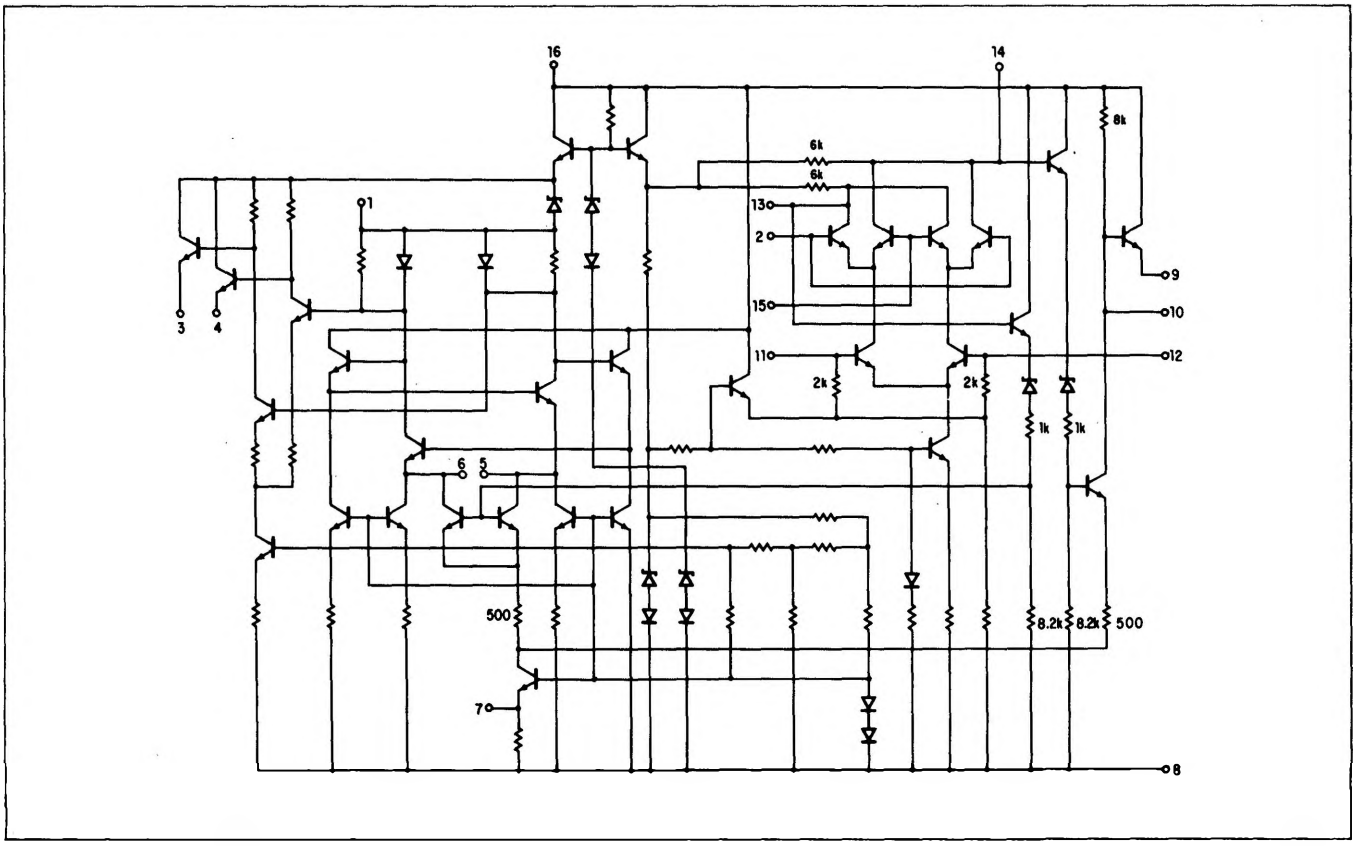
GENERAL ELECTRICAL CHARACTERISTICS

(15,000 ohms pin 9 to ground, 12,000 ohms pins 3 and 4 to ground, pins 2 and 15 to pin 1 through 1000 ohms, input to pin 11 or 12 with unused input at AC ground, range control not connected and V^+ = 18 volts unless otherwise specified. T_A = 25°C.)

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN	TYP	MAX		
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	10	12	14	mA	
Minimum Input Signal for Lock		200		μV	
Dynamic Range		80		dB	
VCO Temp Coefficient*		±0.06	±0.15	%/°C	Measured at 2 MHz
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level	+12	+14	+16	V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		$V_{p\text{-}p}$	Measured at Pin 9
AM Rejection*	30	40		dB	See Definition of Terms
De-emphasis Resistance		8		kΩ	
Bias Reference		+8		V	

*ACC Test Sub Group C.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS (15,000 ohms pin 9 to ground, input to pin 11 or pin 12, AC ground unused input, range control not connected and $V^+ = 18$ volts. $T_A = =25°C$.)

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
10.7 MHz Operation	**Deviation 75 kHz Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	70		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion*		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mV rms Modulation Frequency 1 kHz
4.5 MHz Operation	**Deviation = 25 kHz, Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	60		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Wide Deviation	**$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz Modulation Rate**				
Detection Threshold		1	5	mV	
Demodulated Output		1		V rms	V_{in} = 5 mV rms
Distortion	0.3	0.8		% T.H.D.	V_{in} = 5 mV rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mV rms

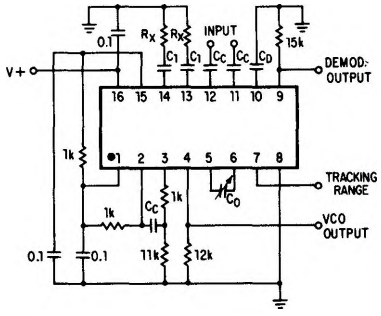
*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS (Input to pin 11 or pin 12, AC ground unused input, range control not connected, $V^+ = 18$ volts. $T_A = 25°C$.)

CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Tracking Range	±5	±15		% of f_o	200 mV p-p square wave input
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		4		V	
VCO Output Impedance		1.3	2.5	kΩ	
VCO Output Swing	3	4.5		V p-p	
VCO Output DC Level		12		V	
VCO Signal/Noise Ratio		60		dB	Inputs at AC ground

TEST CIRCUIT

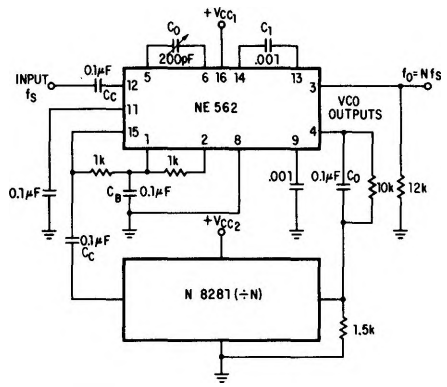
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_D = .01μF for Standard FM
Broadcasting
C_1 and R_x = Low Pass Filter
C_0 = Frequency set Capacitor

FIGURE 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS



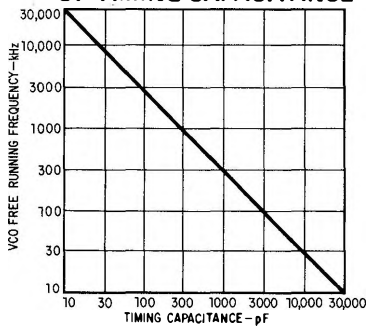
C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = Frequency Capacitor Set

Note: Fanout to divide by N counter is one.

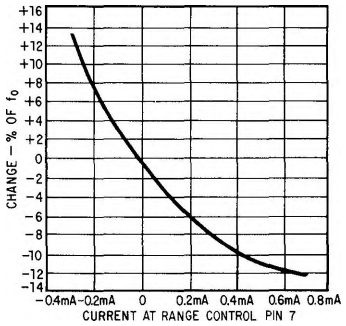
FIGURE 2

TYPICAL CHARACTERISTIC CURVES

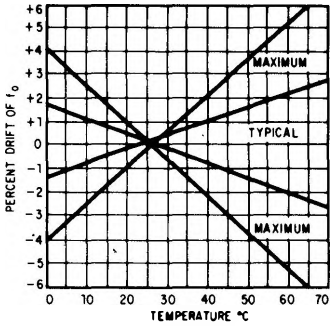
FREE RUNNING VOLTAGE CONTROLLED OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



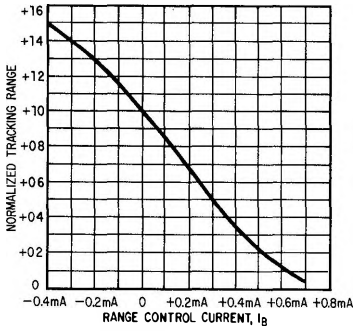
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



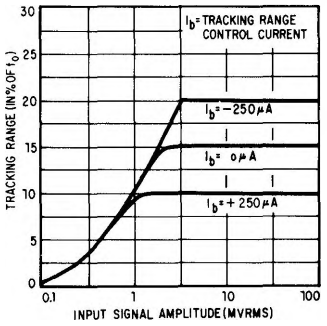
THERMAL DRIFT OF FREE RUNNING FREQUENCY AS A FUNCTION OF TEMPERATURE



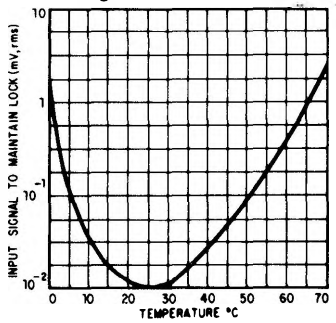
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



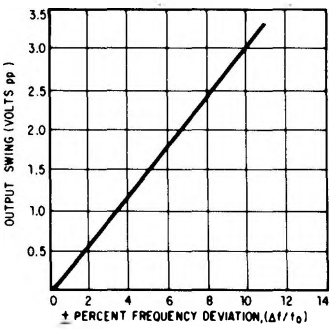
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



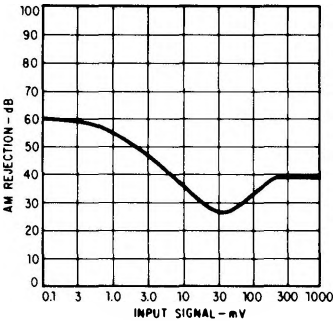
INPUT SIGNAL AMPLITUDE TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE ($f_{signal} = f_o$ = 2.0 MHz)



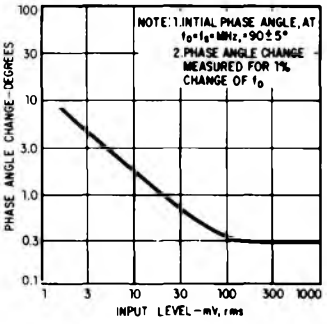
562 PHASE LOCKED LOOP DEMODULATED OUTPUT SWING AS A FUNCTION OF % FM DEVIATION



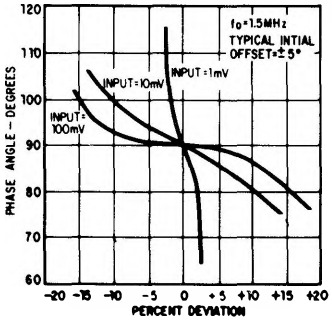
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



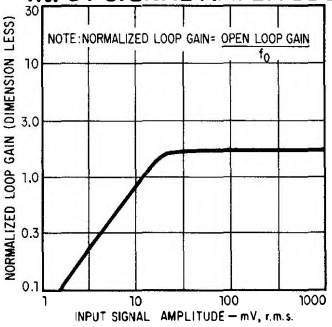
CHANGE IN PHASE ANGLE, f_o RELATIVE TO f_s, AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



VCO OUTPUT PHASE AS A FUNCTION OF PERCENT FREQUENCY DEVIATION



NORMALIZED LOOP GAIN AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



562 APPLICATIONS INFORMATION

1. BIAS REFERENCE

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, Pins 2 and 15. Biasing may be achieved as shown in Figure 3.

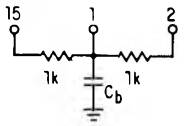


FIGURE 3

2. PHASE COMPARATOR LOOP INPUTS

Of the Signetics high frequency phase locked loops, the 562 is unique in that the loop is open between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a 50% duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a 1000 ohm current limiting buffer resistor should be used in series with the coupling capacitors.

3. VCO OUTPUT

Square wave VCO outputs of both polarities (0°C and 180°C) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4 mA. The output amplitude is typically 4.5 volts peak referenced at +12 volts with respect to pin 8.

4. VCO TUNING

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.

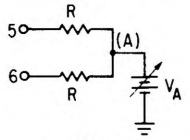


FIGURE 4

The percent change in the VCO free-running frequency, f_o, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to *increase* the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$f = f_o\left[1 - \frac{V_A - 6.4}{1300R}\right]$$

The recommended resistance range of R is 20,000 to 60,000 ohms.

CHANGE IN VCO FREQUENCY AS A FUNCTION OF FINE TUNING VOLTAGE

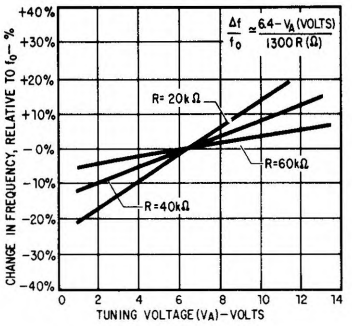


FIGURE 5

5. LOOP GAIN CHARACTERISTICS

The overall open loop gain of the 562 PLL can be expressed as:

$$K_0 = K_1K_2$$

where:

K_0 = total open loop gain

K_1 = phase comparator and amplifier conversion gain

K_2 = VCO conversion gain

The VCO conversion gain, K_2, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$$K_2 = f_o \text{ Hz/Volt}$$

or

$$K_2 = 2\pi f_o \text{ radians/Volt-second}$$

The phase comparator and amplifier conversion gain, K_1, is proportional to input signal amplitude for low input levels, $V_s \leq 40$mV rms, and it is constant and equal to about 1.5 volts/radian for higher input amplitudes. Therefore, K_1 can be approximated as:

$$K_1 \cong \frac{.04\,V_s}{\sqrt{1 + \left(\frac{V_s}{40}\right)^2}}$$

where

V_s = input signal in mV rms.

562 APPLICATIONS INFORMATION (Cont'd.)

6. SIGNAL INPUT

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be bypassed to ground.

7. DEMODULATED OUTPUT

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

8. DE-EMPHASIS FILTER

The de-emphasis terminal, pin 10, is normally required when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3 dB bandwidth of the output amplifier is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is 8000 ohms.

When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be by-passed to ground.

9. TRACKING RANGE CONTROL (Pin 7)

Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of 600Ω.

10. LOW-PASS FILTER

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out of band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating frequencies below 5 MHz, configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the impedance seen looking into the low pass filter terminals, Pins 13 and 14; and, in the 562, is nominally 6000 ohms.

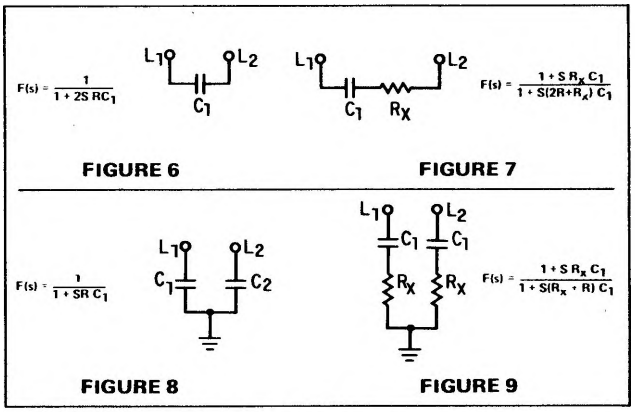


FIGURE 6 FIGURE 7

FIGURE 8 FIGURE 9

11. LOOP GAIN (Threshold) CONTROL

The overall Phase Locked Loop gain can be reduced by connecting a resistor, R_F, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor α, where:

$$\alpha = \frac{R_F}{12{,}000 + R_F}$$

Reduction of loop gain may be desirable at operating frequencies greater than 5 MHz because, at these frequencies, high loop gain may cause instability.

12. STATIC LOOP PHASE-ERROR

When the PLL is in lock, the VCO outputs have a nominal ±90°C phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically ±5°C or less.