54ACTQ574

54ACTQ574 Quiet Series Octal D Flip-Flop with TRI-STATE Outputs



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National Semiconductor

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General Description

The ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable ($\overline{\text{OE}}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (CP) transition.

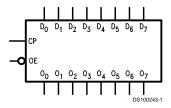
ACTQ574 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series[™] features GTO[™] output control and undershoot corrector in addition to a split ground bus for superior performance.

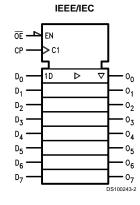
The ACTQ574 is functionally identical to the 'ACTQ374 but with different pin-out.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the ACTQ374
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard ACT574
- 4 kV minimum ESD immunity

Logic Diagrams

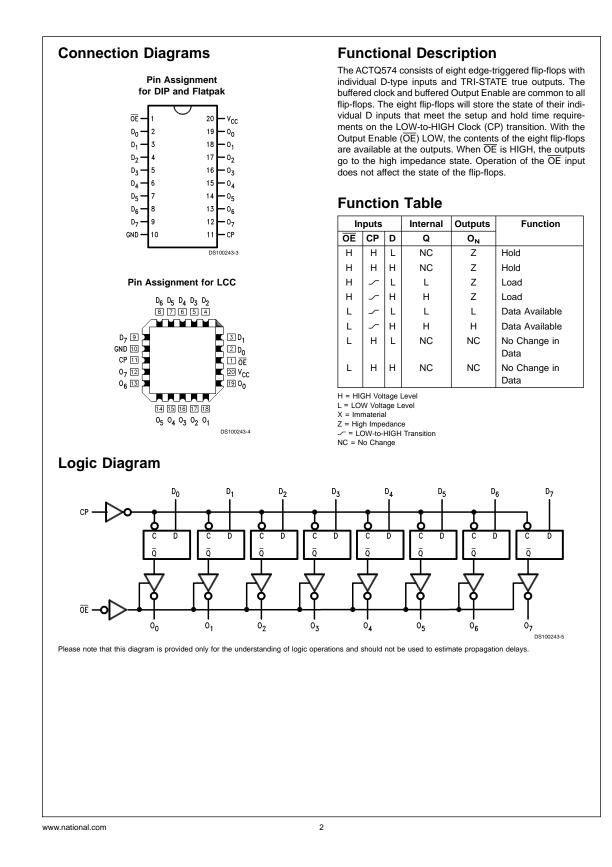




Pin Names	Description	
D ₀ -D ₇	Data Inputs	
CP	Clock Pulse Input	
ŌĒ	TRI-STATE Output Enable Input	
0 ₀ -0 ₇	TRI-STATE Outputs	

 $\label{eq:GTO} GTO^{IV} is a trademark of National Semiconductor Corporation. \\ TRI-STATE® is a registered trademark of National Semiconductor Corporation. \\ FACT® is a registered trademark of Fairchild Semiconductor Corporation. \\ FACT Quiet Series^{IV} is a trademark of Fairchild Semiconductor Corporation. \\$

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (IIK)	
$V_{I} = -0.5V$	–20 mA
$V_{I} = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (VI)	-0.5V to V _{CC} + 0.5V
DC Output Diode Current (I _{OK})	
$V_{O} = -0.5V$	–20 mA
$V_{O} = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V _O)	–0.5V to V _{CC} + 0.5V
DC Output Source	
or Sink Current (I _O)	±50 mA
DC V _{CC} or Ground Current	
per Output Pin (I _{CC} or I _{GND})	±50 mA
Storage Temperature (T _{STG})	–65°C to +150°C
DC Latch-Up Source or	
Sink Current	±300 mA
Junction Temperature (T_J)	

Recommended Operating Conditions

CDIP

Supply Voltage (V _{CC})		
'ACTQ	4.5V to 5.5V	
Input Voltage (V _I)	0V to V_{CC}	
Output Voltage (V _O)	0V to V_{CC}	
Operating Temperature (T _A)		
54ACTQ	–55°C to +125°C	
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACTQ Devices		
V _{IN} from 0.8V to 2.0V		
V _{CC} @ 4.5V, 5.5V	125 mV/ns	
Note 1: All commercial packaging is not recomme quiring greater than 2000 temperature cycles from		
Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT TM circuits outside databook specifications.		

175°C

DC Electrical Characteristics for 'ACTQ Family Devices

			54ACTQ	Units	Conditions
Symbol	Parameter	V _{cc}	T _A =		
		(V)	-55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level	4.5	2.0	V	V _{OUT} = 0.1V
	Input Voltage	5.5	2.0		or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level	4.5	0.8	V	V _{OUT} = 0.1V
	Input Voltage	5.5	0.8		or $V_{CC} - 0.1V$
V _{он}	Minimum High Level	4.5	4.4	V	Ι _{ΟUT} = -50 μΑ
	Output Voltage	5.5	5.4		
					(Note 3)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	3.70	V	I _{он} = –24 mA
		5.5	4.70		I _{он} = –24 mA
V _{OL}	Maximum Low Level	4.5	0.1	V	Ι _{ΟUT} = 50 μΑ
	Output Voltage	5.5	0.1		
					(Note 3)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	0.50	V	I _{OL} = 24 mA
		5.5	0.50		I _{OL} = 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_{I} = V_{CC}, GND$
l _{oz}	Maximum TRI-STATE	5.5	±5.0	μA	$V_{I} = V_{IL}, V_{IH}$
	Leakage Current				$V_{O} = V_{CC}, GND$
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	$V_{I} = V_{CC} - 2.1V$
I _{OLD}	(Note 4)	5.5	50	mA	V _{OLD} = 1.65V Max
	Minimum Dynamic				
I _{OHD}	Output Current	5.5	-50	mA	V _{OHD} = 3.85V Min
I _{cc}	Maximum Quiescent	5.5	80.0	μA	$V_{IN} = V_{CC}$
	Supply Current				or GND (Note 5)

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

			54ACTQ			
Symbol			V_{CC} $T_{A} =$ (V) -55°C to +125°C		Conditions	
			Guaranteed Limits			
V _{OLP}	Quiet Output	5.0	1.5	V	(Notes 6, 7)	
	Maximum Dynamic V _{OL}					
V _{OLV}	Quiet Output	5.0	-1.2	V	(Notes 6, 7)	
	Minimum Dynamic V _{OL}					

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 6: Plastic DIP package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 8: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

	Parameter		54A	Units	
Symbol		V _{cc} (V)	T _A = to +'		
		(Note 9)	C _L =	50 pF Max	-
f _{max}	Maximum Clock Frequency	5.0	95	max	MHz
t _{PLH} , t _{PHL}	Propagation Delay CP to \overline{O}_n	5.0	1.0	11.0	ns
t _{PZH} , t _{PZL}	Output Enable Time	5.0	1.0	11.0	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.0	10.0	ns

Note 9: Voltage Range 5.0 is 5.0V ±0.5V.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

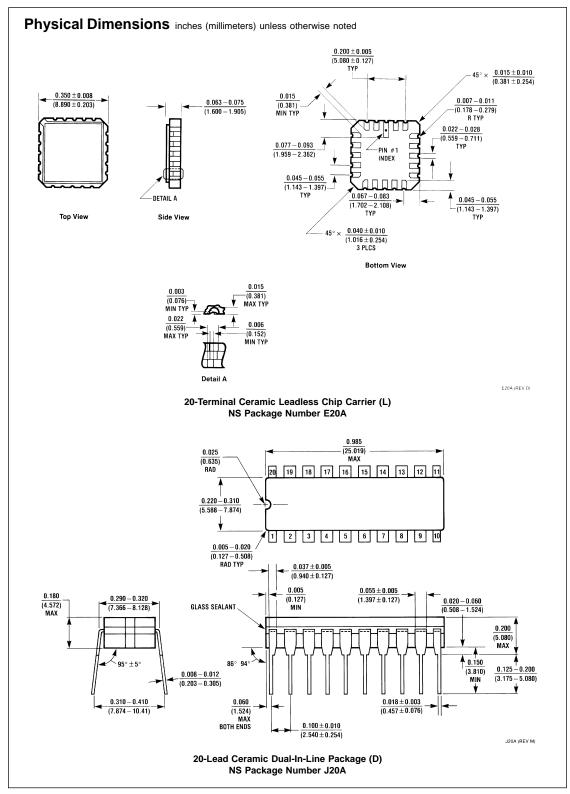
AC Operating Requirements

			54ACTQ		
		V _{cc}	T _A = -55°C	Units	
Symbol	Parameter	(V)	to +125°C		
		(Note 11)	C _L = 50 pF		
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW	5.0	3.5	ns	
	D _n to CP				
t _H	Hold Time, HIGH or LOW	5.0	2.0	ns	
	D _n to CP				
t _w	CP Pulse Width,	5.0	5.0	ns	
	HIGH or LOW				

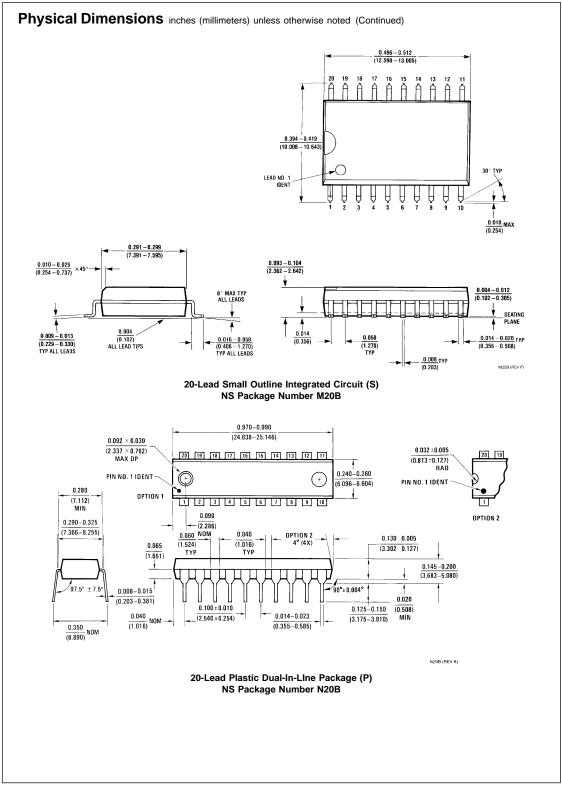
Note 11: Voltage Range 5.0 is 5.0V $\pm 0.5V$

mbol	Parameter	Тур	Units	Conditions
	Input Capacitance	4.5	pF	V _{CC} = OPEN
	Power Dissipation Capacitance	40.0	pF	$V_{\rm CC} = 5.0 V$

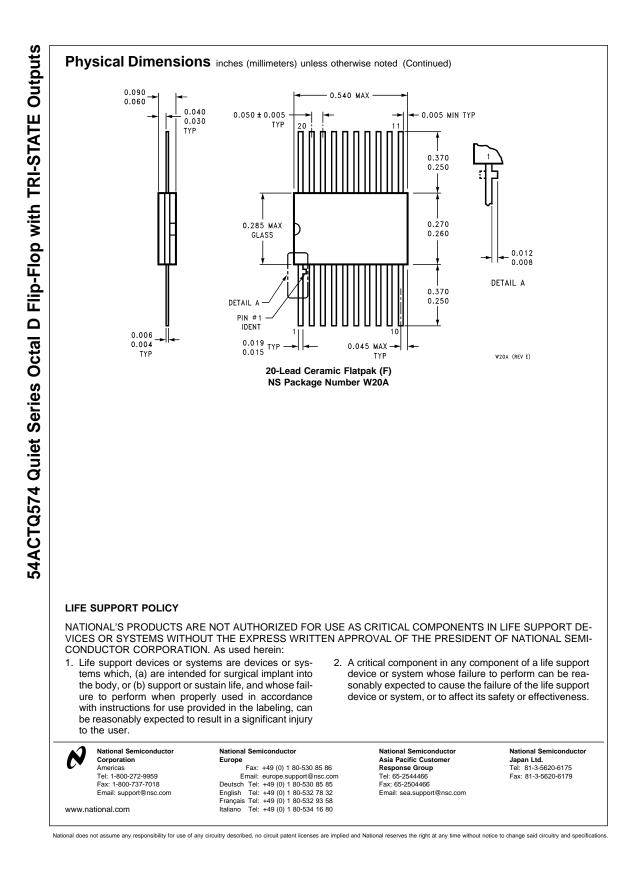
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