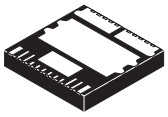
MC33982PNATAD
Rev 4.0, 5/2012

Single Intelligent High-Current Self-Protected Silicon High-Side Switch

33982

High-Side Switch



98ARL10521D
16-TERMINAL PQFN
12 mm x 12 mm

Note For package dimensions, refer to 98ARL10521D.

Thermal Addendum

Introduction

This thermal addendum is provided as a supplement to the MC33982 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

This package is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

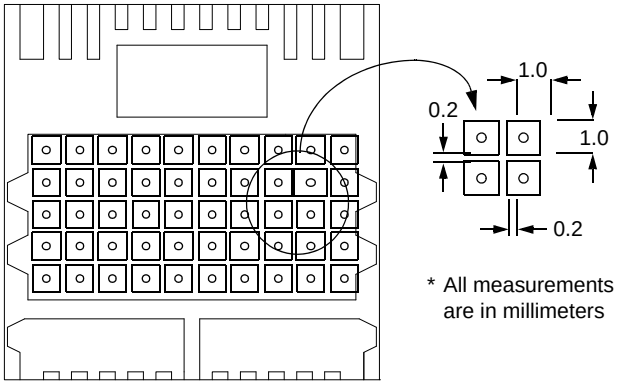
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1), (2)	20	16	39
$R_{\theta JBmn}$ (2), (3)	6	2.0	26
$R_{\theta JAmn}$ (1), (4)	53	40	73
$R_{\theta JCmn}$ (5)	<0.5	0.0	1.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



Note: Recommended via diameter is 0.5 mm. PTH (plated through hole) via must be plugged / filled with epoxy or solder mask in order to minimize void formation and to avoid any solder wicking into the via.

Figure 1. Surface Mount for Power PQFN with Exposed Pads

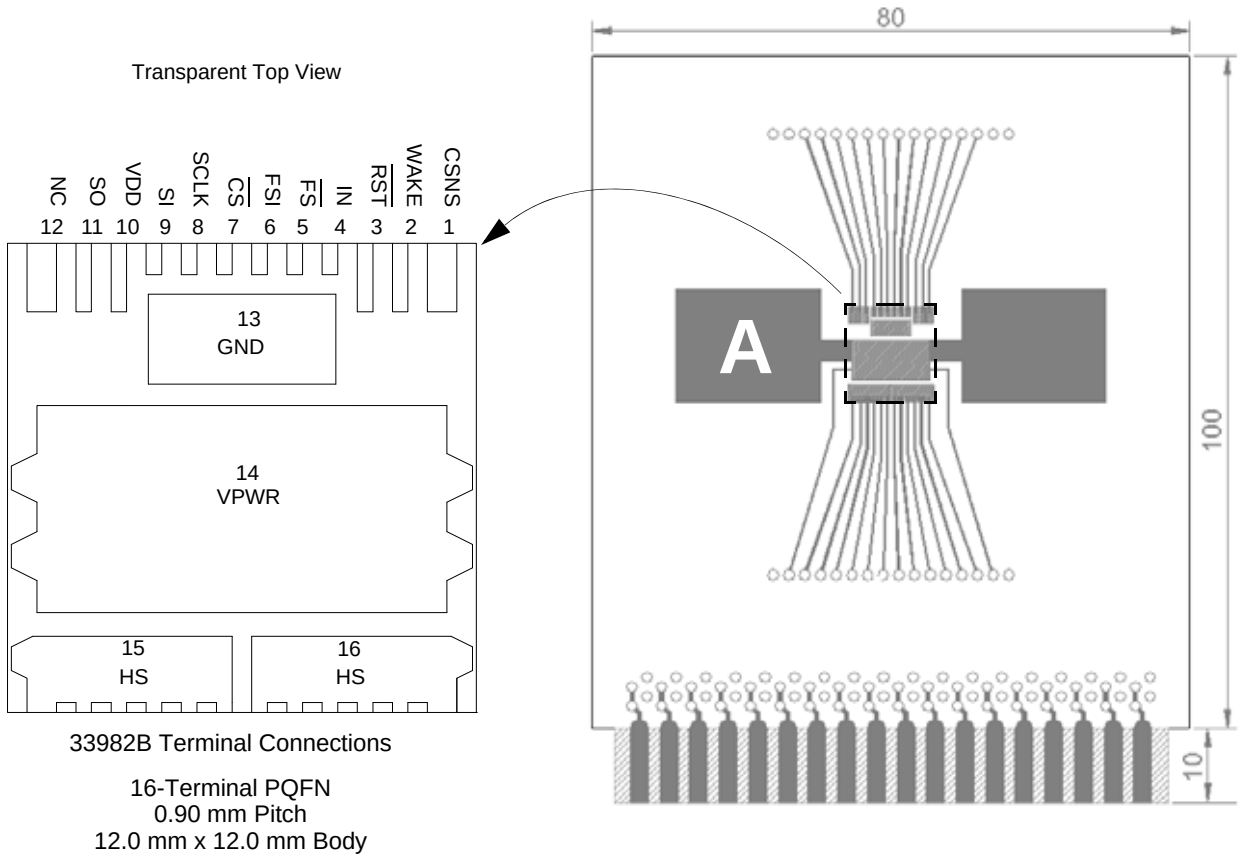


Figure 2. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 2. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	55	42	74
	300	41	32	66
	600	39	29	65

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

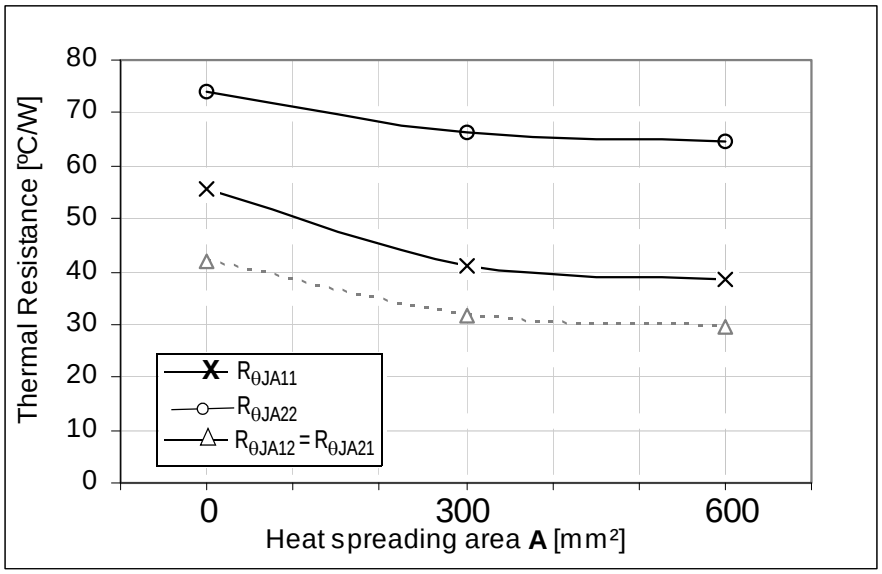


Figure 3. Device on Thermal Test Board $R_{\theta JA}$

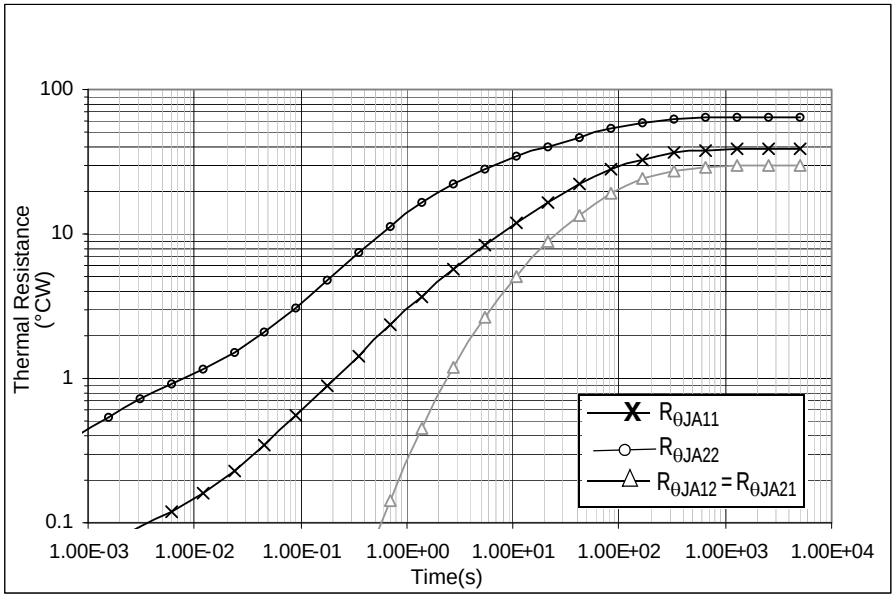


Figure 4. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

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