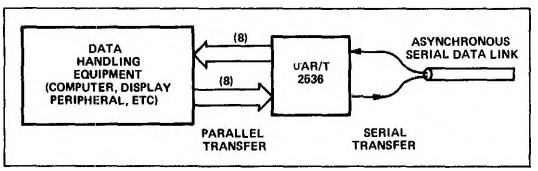
Signetics

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UAR-T) 2536

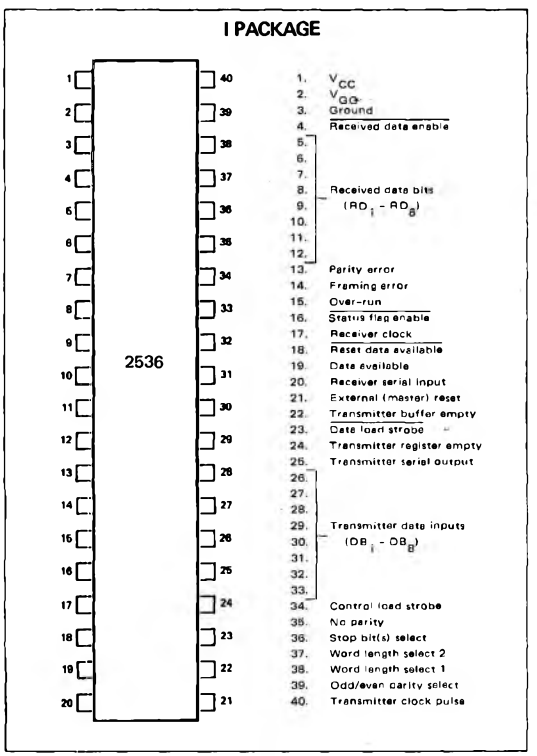
PRELIMINARY SPECIFICATION — SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2536 Universal Asynchronous Receiver-Transmitter is a general purpose, programmable MOS/LSI subsystem integrated on a single monolithic chip. The device can simultaneously convert asynchronous serial binary characters to a parallel format (receiver) and parallel binary characters to serial, asynchronous output (transmitter) with start, parity, and stop bits added or verified. Both receiver and transmitter are double buffered and fully compatible with bipolar logic. The UAR-T may be programmed as follows: the word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited; the parity may be even or odd; and the number of stop bits may be either one or two. The 2536 is pin compatible with the TMS 6010, AY-5-1012, TR-1402A, S1757 & COM2502.



PIN CONFIGURATION (Top View)



FEATURES

- DIRECTLY TTL/DTL COMPATIBLE - NO INTERFACING CIRCUITS REQUIRED
- FULL DUPLEX OR HALF DUPLEX OPERATION - TRANSMITS AND RECEIVES DATA SIMULTANEOUSLY OR ALTERNATELY (AT INDEPENDENT INFORMATION RATES)
- FULLY BUFFERED - ELIMINATES NEED FOR SYSTEM SYNCHRONIZATION: FACILITATES HIGH SPEED OPERATION.
- FULLY PROGRAMMABLE - EXTERNALLY SELECTABLE:
  - WORD LENGTH: 5, 6, 7, 8 DATA BITS
  - INFORMATION RATE - UP TO 20K BAUD
  - EVEN/ODD PARITY
  - PARITY INHIBIT
  - SINGLE OR DOUBLE STOP BIT GENERATION
- AUTOMATIC DATA STATUS GENERATION:
  - TRANSMISSION COMPLETE
  - TRANSMITTER BUFFER REGISTER EMPTY
  - RECEIVED DATA AVAILABLE
  - PARITY ERROR
  - FRAMING ERROR
  - OVERRUN ERROR
- THREE-STATE OUTPUTS, RESETABLE - BUSSING CAPABILITY:
  - DATA OUTPUTS
  - STATUS FLAGS
- INTERNAL PULL-UPS ON ALL INPUTS
- CLOCK BITS TO DATA BITS RATIO - 16 OPTIONS AVAILABLE- 32, (8, 4, 2)
- HIGH SPEED OPERATION - FROM D.C. TO 320KHz GUARANTEED
- START BIT VERIFICATION-MINIMIZES ERROR RATE
- STATIC LOGIC - STABLE
- STANDARD POWER SUPPLIES - +5V, −12V
- DUAL IN-LINE PACKAGE - CERAMIC

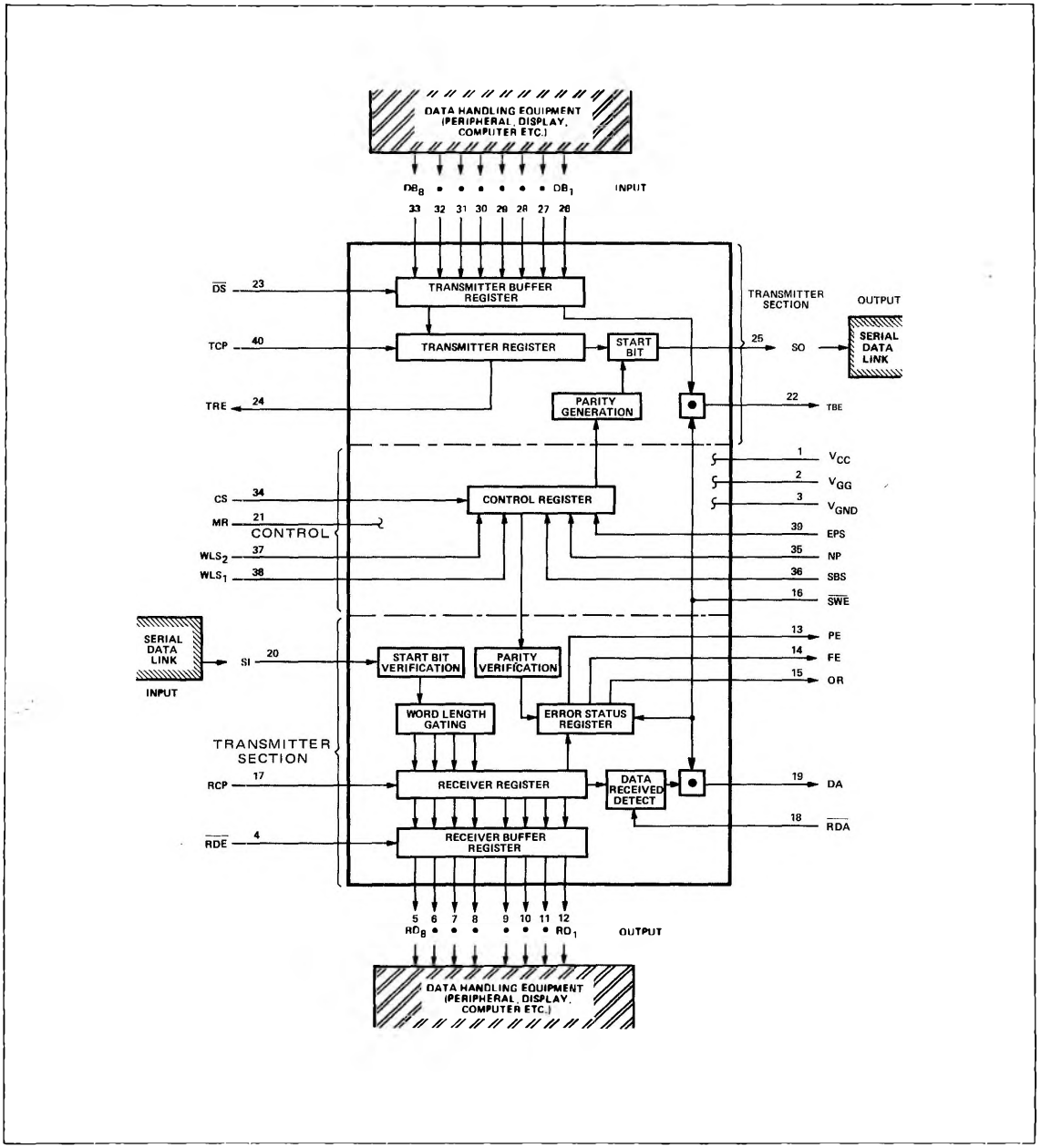
APPLICATIONS

PERIPHERALS	MULTIPLEXERS
TERMINALS	CONTROLLERS
PRINTERS	CARD AND TAPE READERS
MINI-COMPUTERS	KEYBOARD ENCODERS
MODEMS	REMOTE DATA ACQUISITION
CONCENTRATORS	SYSTEMS

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP RANGE
2536 I	40-Pin Ceramic DIP	0-70°C

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

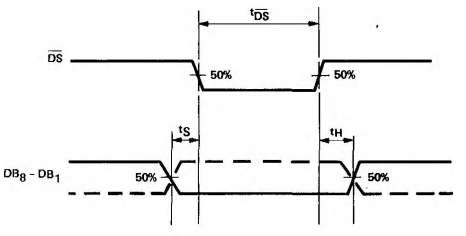
		Package Power Dissipation (2) @T_A = 70°C	3.0W(14)
Operating Ambient Temperature	0°C to 70°C	Input (3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V
Storage Temperature	-65°C to +150°C		

DC CHARACTERISTICS

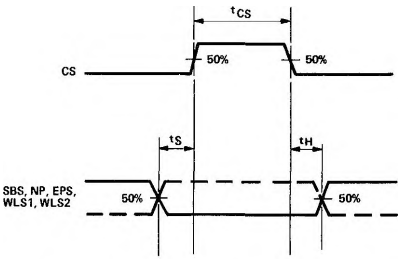
T_A = 0°C to 70°C, V_{CC} = 5V (8), V_{DD} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7, 8)

SYMBOL	TEST	MIN	TYP	MAX	UNIT.	CONDITIONS
V_{IH}	Input "High" Voltage (9)	3.2		5.3	V	
V_{IL}	Input "Low" Voltage			1.05	V	
$V_{IH\phi}$	Clock Input "High" Voltage (9)	3.2		5.3	V	
$V_{IL\phi}$	Clock Input "Low" Voltage			1.05	V	
I_{IH}	Input "High" Current			10	ua	V_{IN} = 5.0V
I_{IL}	Input "Low" Current			1.6	ma	V_{IN} = 0V
$I_{IH\phi}$	Clock Input "High" Current			10	ua	V_{IN} = 5.0V
$I_{IL\phi}$	Clock Input "Low" Current			1.6	ma	V_{IN} = 0V
I_{CC}	V_{CC} Supply Current		20		ma	All Inputs Logic "High"
I_{GG}	V_{GG} Supply Current		10		ma	All Inputs Logic "High"
P_D	Power Dissipation		200		mW	All Inputs Logic "High"

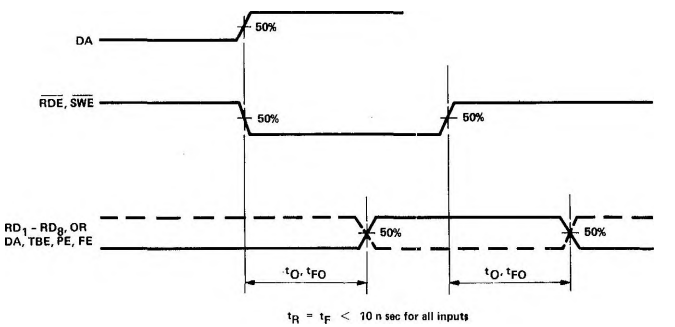
TIMING DIAGRAM AND VOLTAGE WAVEFORMS



TRANSMITTER DATA INPUT LOAD CYCLE



CONTROL REGISTER LOAD CYCLE



$t_R = t_F < 10$ n sec for all inputs

OUTPUT DELAYS

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V(8), V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7, 8, 10, 11, 13)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
f_C	Clock Frequency (12)	DC	480	320	KHz	
BR	Baud Rate		30	20	kBaud	(Clock/Data ratio = 16)
$t_{PW\phi}$	Clock Pulse Width	1.5	1.0	100	us	
$t_{PW\overline{\phi}}$	$\overline{\text{Clock}}$ Pulse Width	1.5	1.0	DC	us	
$t_{\overline{DS}}$	$\overline{\text{Data}}$ Strobe Width	200			ns	
t_{CS}	Control Strobe Width	200			ns	
t_{MR}	Master Reset Pulse Width	1.0			us	
$t_{\overline{RDA}}$	Receiver Data Available Reset Pulse Width	300			ns	
$t_{\overline{RDE}}$	Receiver Data Enable Pulse Width	400			ns	
$t_{\overline{SWE}}$	Status Word Enable Pulse Width	400			ns	
t_{NP}	Parity Inhibit Pulse Width (11)	400			ns	
t_{EPS}	Even/Odd Parity Pulse Width (11)	400			ns	
t_{SBS}	Stop Bit Select Pulse Width (11)	400			ns	
T_{WLS}	Word Length Select Pulse Width (11)	400			ns	
t_S	Data and Control Set-up Time	10			ns	
t_H	Data and Control Hold Time	20			ns	
t_{RR}	Receiver Reset Delay (RDA to DA)		0.5		us	
t_{FO}	Flag Output Delay (SWE to Flag)	0.3			us	
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL Load (I_{OUT} = 1.6ma)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL Load (I_{OUT} = -100ua)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	
t_{OL}	Receiver Output Logic "Low" Delay		300	500	ns	1 TTL Load
t_{OH}	Receiver Output Logic "High" Delay		300	500	ns	1 TTL Load
C_{IN}	Input Capacitance (all inputs)			10	pF	@1MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Input Capacitance			10	pF	@1MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150° C maximum junction temperature and a thermal resistance of 50° C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25° C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. The 2536 is equipped with an internal pull-up device on all input terminals to enhance the "1" level of driving TTL gate. The pull-up impedance is typically 10K ohms to V_{CC}.
10. Output load capactiance 20pF max.
11. Input rise and fall times 10ns. Output load is one standard TTL gate.
12. Clock frequency is 16 times Baud rate for a standard 2536.
13. NP, EPS, WLS1, WLS2, and SGS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
14. Note that this figure is the maximum dissipation allowed in this package. Actual device power dissipation can be found in the D.C. Characteristics Table.

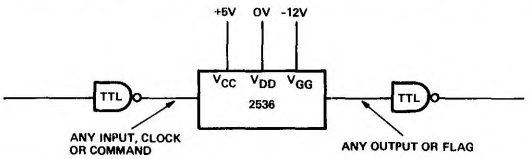
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	-12V Supply
3	Ground	V_{GND}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "O" input enables the outputs (RD_8-RD_1) of the receiver buffer register.
5-12	Receiver Data Outputs	RD_8 - RD_1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD_1. These lines have resettable three-state outputs; i.e., they have normal TTL output characteristics when $\overline{RDE}$ is "O" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be "bus" structured. Unused data output lines, as selected by WLS_1 and WLS_2, have a "O" output.
13	Receiver Parity Error	PE	This three-state output (enabled by "O" on $\overline{SWE}$) goes to a logic "1" if the received character parity bit does not agree with the selected parity.
14	Receiver Framing Error	FE	This three-state output (enabled by "O" on $\overline{SWE}$) goes to a logic "1" if the received character does not have a valid stop bit.
15	Receiver Over-Run Error	OR	This three-state output (enabled by "O" on $\overline{SWE}$) goes to a logic "1" if the previously received character is not read (DA output not reset with $\overline{RDA}$) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "O" on this line enables three-state outputs (PE, FE, OR, DA, TBE) of the status buffer register.
17	Receiver Clock	RCP	Receiver clock line input. Frequency is 16 times (16X) the desired receiver baud rate. Other versions available on special order (contact Signetics) (32X, 8X, 4X, 2X).
18	Reset Data Available	$\overline{RDA}$	A logic "O" will reset the DA line to a "O".
19	Receiver Data Available	DA	This three-state output (enabled by "O" on $\overline{SWE}$ goes to a logic "1" when an entire character has been received and transferred to the receiver buffer register.
20	Receiver Serial Input	SI	This input accepts the serial bit input stream into receiver register at a point determined by the character length, parity, and the number of stop bits. A Mark (logic "1") to Space (logic "O") transition is required for initiation of data reception. A logic "1" must be present when data is not being received.
21	External (Master) Reset	MR	This line is strobed to a logic "1" to clear the logic after power turn-on. It resets all registers and sets the transmitter serial output line, SO and all three-state outputs to a logic "0".
22	Transmitter Buffer Empty	TBE	The transmitter buffer empty flag (enabled by "O" on $\overline{SWE}$) goes to a logic "1" when the transmitter buffer register has transferred its content to the transmitter register and may be loaded with a new character.
23	Transmitter Data Strobe	$\overline{DS}$	A "O" strobe on this line enters a character into the transmitter buffer register. A rising (positive) edge transition of that strobe transfers the character into the transmitter register if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is transferred simultaneously with the initiation of its serial transmission (start bit).

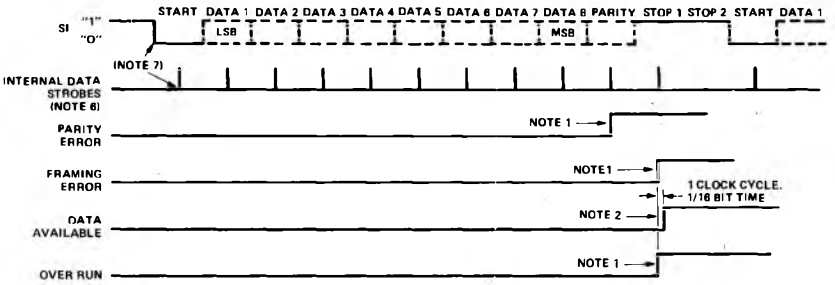
DESCRIPTION OF PIN FUNCTIONS (Cont'd)

PIN NO.	NAME	SYMBOL	FUNCTION
24	Transmitter End of Character	TRE	A logic "1" on this output indicates that the transmitter register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	Transmitter Serial Output	SO	The content of the transmitter register (start bit, data bits, parity bit, and stop bit(s)), are serially shifted out on this line. It will remain at logic "1" when no data is being transmitted. A start of transmission is defined as the transition from logic "1" to a logic "0" of the start bit.
26-33	Transmitter Data	DB_1 - DB_8	There are 8 data input lines (strobed by DS) available. Unused data input lines, as selected by WLS1 and WLS2, may be in either logic state. The LSB should always be placed on DB_1. A logic "1" input will cause a logic "1" output to be transmitted.
34	Control Strobe	CS	A "1" strobe on this line enters the control bits (EPS, NP, SBS, WLS2, and WLS1) into the control register. This line may be strobed or hard-wired to a logic "1" level.
35	Parity Inhibit	NP	A logic "1" on this line inhibits the parity generation and verification circuits. It clamps the PE line to a logic "0". The stop bit(s) will immediately follow the last data bit. If not used, this line must be tied to a logic "0".
36	Number of Stop Bits Select	SBS	This line selects the number of stop bits (logic "1") generated after a parity bit during transmission. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Data Bits/ Character Select	WLS1 WLS2	These two lines will be internally decoded to select either 5, 6, 7, or 8 data bits per character. WLS1 / WLS2 / Bits/Character 0 / 0 / 5 1 / 0 / 6 0 / 1 / 7 1 / 1 / 8
39	Odd/Even Parity Select	EPS	The logic level on this pin, in conjunction with the NP input, selects the t ype of parity mode which will be generated by the transmitter and checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock	TCP	Transmitter clock line input. Frequency is 16 times (16X) the desired baud rate. Note: other versions are available on special order (32X, 8X, 4X, 2X).

TTL INTERFACE CIRCUIT



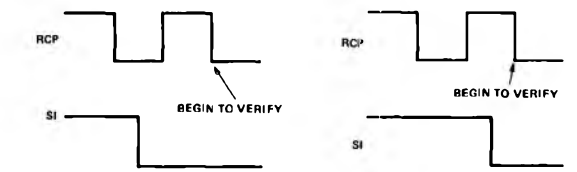
UAR-T RECEIVER OPERATION TIMING DIAGRAM



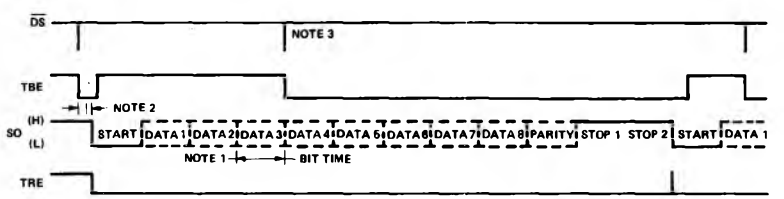
NOTES:

1. This is the time when the error conditions are detected, if error occurs.
2. Data available is set only when the received data PE, FE, OR has been transferred to the buffer registers.
3. All information is good in buffer register until date available tries to set for next character.
4. Above shown for 8 level code parity and two stop for no parity stop bits follow date.
5. For all level codes, the data in the holding register is right justified; that is, LSB always appears in RD1 (Pin 12).
6. These data strobes are internally generated to sample at the center of a bit.
7. If the receiver serial input (SI) line remains "Spacing" (Logic "O") for 1/2 a bit time, a genuine start bit is verified. Should the line return to a "Marking" condition (logic "1") prior to a 1/2 of a bit time, the start bit verification process will be reset (invalid start bit). See Detail.

DETAIL



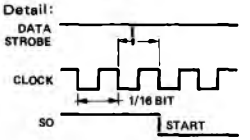
UAR-T TRANSMITTER OPERATION TIMING DIAGRAM



NOTE: Transmitter initially assumed inactive at start of diagram. Shown for 8 level code and parity and two stops.

1. Bit Time = 16 clock cycles.
2. If transmitter is inactive the start pulse will appear on line within 1 clock cycle of time data strobe occurs. See detail.
3. Since transmitter is double buffered another data strobe can occur anywhere during transmission of character 1.

Detail:



RECEIVER OPERATION

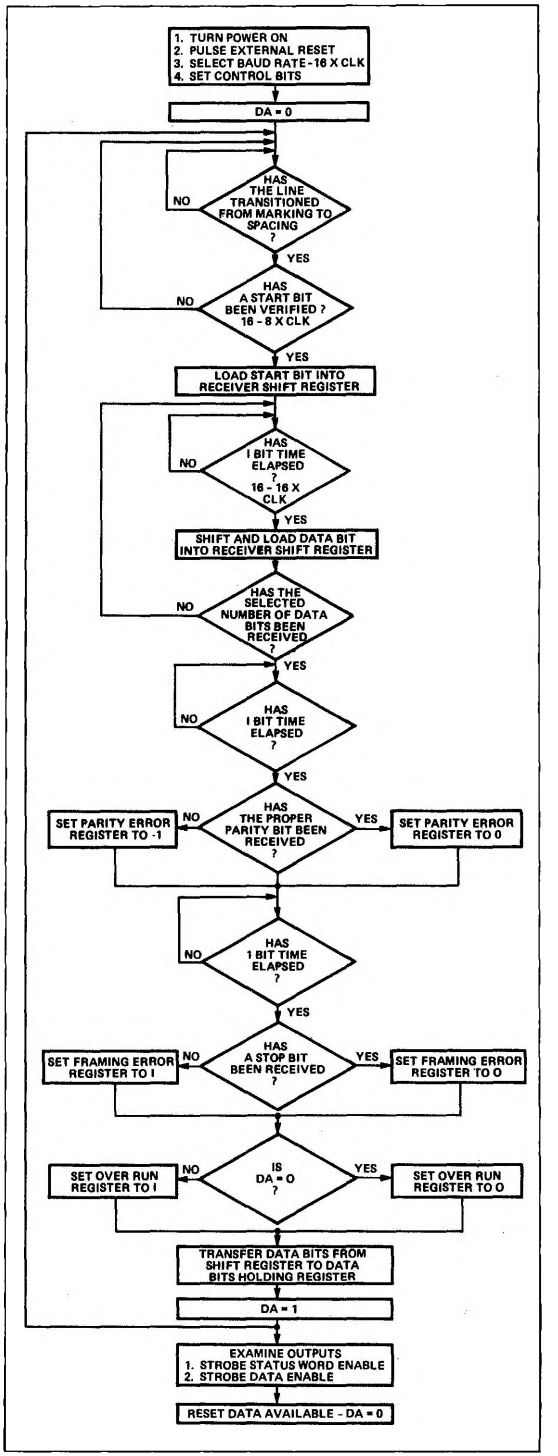
INITIALIZING

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "O".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to Spacing (logic "O") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "O", the SI line continues to be at logic "O", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "O" (Marking to Spacing) when the 16X clock is in logic "1" state, the bit time for center sampling, will begin when the clock line transitions from a logic "1" to a logic "O" state. After verification of a genuine start bit, data bit reception, parity bit reception, and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected, the PE (parity error) will be set to a logic "O"

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status buffer register will be set to a logic "1". If the DA signal is at a logic "O", the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



TRANSMITTER OPERATION

INITIALIZING

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBE, TRE, and SO to logic "1" (line is Marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed, the TBE signal will change from a logic "1" to a logic "O" indicating that the data bits buffer register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. When transmitter shift register is empty, data bits in the buffer register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and TRE going to a logic "O", and TBE will also go to a logic "1" indicating that the shifting operation is completed and that the data bits buffer register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits buffer register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, TRE will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBE is a logic "O" as was previously discussed.