signetics

12-BIT PARITY CHECKER-GENERATOR CIRCUIT

10160

ADVANCE INFORMATION
TO BE ANNOUNCED

10160 F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10160 is a high performance parity circuit constructed with nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation.

Input pulldown resistors ensure that the unconnected inputs are pulled to low logic level allowing parity detection and generation for less than 12 bits.

The Output goes high with ODD parity on input pins 3 through 15. (That is, if there are 1,3,5,7,9 or 11 '1's on these inputs).

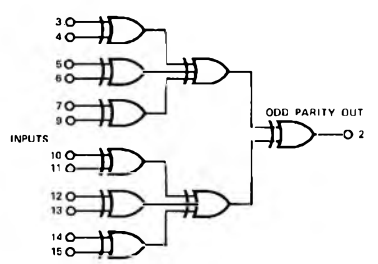
Expansion for word lengths greater than 12 bits can be achieved by connecting to the carry inputs of the 10170 Parity Circuit or by using 10107 or 10113 EXCLUSIVE-OR gates.

FEATURES

- HIGH FUNCTIONAL DENSITY ON ONE CHIP REDUCES PACKAGE COUNT AND SAVES SYSTEM POWER
- FAST PROPAGATION DELAY = 4.0 ns TYP
- LOW POWER DISSIPATION = 325 mW/PACKAGE TYPE (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- CONTROLLED OUTPUT RISE AND FALL TIMES –2.0 ns TYP (20% TO 80%)(ALL OUTPUTS LOADED)
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

LOGIC DIAGRAM

10160



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

ELECTRICAL CHARACTERISTICS

Conditions: T_A = 25°C, V_{EE} = −5.2 V ±1%

1. I_E = 62 mA dc typ.
   = 78 mA dc max.
2. I_{inH} = 265 μA dc max. (pin 3 etc.)
   = 220 μA dc max. (pin 4 etc.)

Conditions: T_A = 25°C, V_{CC} = +2.0 V ±1%, V_{EE} = −3.2 V ±1%, 50 Ω loads

3. t_{pd} = 4.0 ns typ.
4. t_r, t_f = 2.0 ns typ. (20% to 80%)

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP