# signetics

# DUAL MULTIPLEXER - LATCH (WITH INDEPENDANT SELECTS) 10134

10134F: –30 to +85°C CERDIP

## DIGITAL 10,000 SERIES ECL

## DESCRIPTION

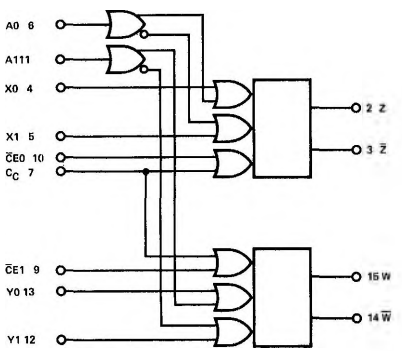
The 10134 is a dual clocked D-type latch with 2 to 1 data multiplexing. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this state, the enable inputs perform the function of enabling the common clock ($C_C$).

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

## LOGIC DIAGRAM

10134




$V_{CC1}$ = 1, $V_{CC2}$ = 16, $V_{EE}$ = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

## FEATURES

- HIGH SPEED COMBINED MULTIPLEXER – LATCH IMPROVES SYSTEM PERFORMANCE.
- MULTIPLEXED INPUTS TO REDUCE PACKAGE COUNT
- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA)
  = 3.5 ns TYP (SELECT)
  = 4.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 225 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: $V_{EE}$ = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

## APPLICATIONS

- COMBINED MULTIPLEXER – REGISTER FOR:
  - high speed central processors
  - high speed peripherals
  - high speed minicomputers
  - high speed accumulators
  - communication systems

## TRUTH TABLE

| C | A0 | X0 | X1 | $Z_{n+1}$ |
|---|---|---|---|---|
| L | L | L | ϕ | L |
| L | L | H | ϕ | H |
| L | H | ϕ | L | L |
| L | H | ϕ | H | H |
| H | ϕ | ϕ | ϕ | $Z_n$ |

ϕ = Don't Care
$C = \overline{CE} + C_C$
$X_{in} = \overline{A0} \cdot X0 + A0 \cdot X1$

## TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

## PACKAGE TYPE

- F: 16-Pin CERDIP

## ELECTRICAL CHARACTERISTICS

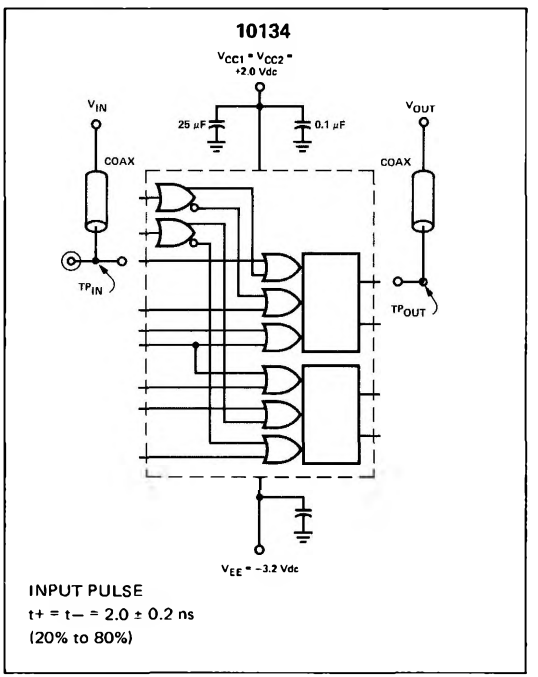
**(At Listed Voltages and Ambient Temperatures).**

| @ Test Temperature | TEST VOLTAGE VALUES (Volts) $V_{IH}$ max | $V_{IL}$ min | $V_{IHA}$ min | $V_{ILA}$ max | $V_{EE}$ |
|---|---|---|---|---|---|
| −30°C | −0.890 | −1.890 | −1.205 | −1.500 | −5.2 |
| +25°C | −0.810 | −1.850 | −1.105 | −1.475 | −5.2 |
| +85°C | −0.700 | −1.625 | −1.035 | −1.440 | −5.2 |

| Characteristic | Symbol | Pin Under Test | 10134 Test Limits −30°C Min | −30°C Max | +25°C Min | +25°C Max | +85°C Min | +85°C Max | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH}$ max | $V_{IL}$ min | $V_{IHA}$ min | $V_{ILA}$ max | $V_{EE}$ | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 8 | – | – | – | 55 | – | – | mAdc | 6,7,11 | – | – | – | 8 | 1,16 |
| Input Current | $I_{in\ H}$ | 4 | – | – | – | 290 | – | – | µAdc | 4 | – | – | – | 8 | 1,16 |
| | | 5 | – | – | – | 290 | – | – | | 5,6 | – | – | – | | |
| | | 6 | – | – | – | 220 | – | – | | 6 | – | – | – | | |
| | | 7 | – | – | – | 290 | – | – | | 7 | – | – | – | | |
| | | 10 | – | – | – | 220 | – | – | | 10 | – | – | – | | |
| | $I_{in\ L}$ | 4* | – | – | 0.50 | – | – | – | µAdc | – | 4 | – | – | 8 | 1,16 |
| Logic "1" Output Voltage | $V_{OH}$ | 2 | −1.060 | −0.890 | −0.960 | −0.810 | −0.890 | −0.700 | Vdc | 4 | 6,7,10 | – | – | 8 | 1,16 |
| | | 2 | −1.060 | 0.890 | 0.960 | 0.810 | −0.890 | −0.700 | Vdc | 5,6 | 7,10 | – | – | 8 | 1,16 |
| Logic "0" Output Voltage | $V_{OL}$ | 2 | −1.890 | −1.675 | −1.850 | −1.650 | −1.825 | −1.615 | Vdc | – | 4,6,7,10 | – | – | 8 | 1,16 |
| | | 2 | −1.890 | −1.675 | −1.850 | −1.650 | −1.825 | −1.615 | Vdc | 6 | 5,7,10 | – | – | 8 | 1,16 |
| Logic "1" Threshold Voltage | $V_{OHA}$ | 2 | −1.060 | – | −0.980 | – | −0.910 | – | Vdc | – | 6,7,10 | 4 | – | 8 | 1,16 |
| | | 2 | −1.080 | – | −0.980 | – | −0.910 | – | Vdc | 6 | 7,10 | 5 | – | 8 | 1,16 |
| Logic "0" Threshold Voltage | $V_{OLA}$ | 2 | – | −1.655 | – | −1.630 | – | −1.595 | Vdc | – | 6,7,10 | – | 4 | 8 | 1,16 |
| | | 2 | – | −1.655 | – | −1.630 | – | −1.595 | Vdc | 6 | 7,10 | – | 5 | 8 | 1,16 |
| Switching Times (50-ohm load) (See Figure 1) | | | | | Typ | Max | | | | +1.11 V | +0.31 V | Pulse In | Pulse Out | −3.2 V | +2.0 V |
| Propagation Delay Data | $t_{4+2+}$ | 2 | – | – | 2.5 | – | – | – | ns | – | 6,7,10 | 4 | 2 | 8 | 1,16 |
| Clock | $t_{10-2+}$ | | – | – | 4.0 | – | – | – | | 4 | 7 | 10 | | | |
| Select | $t_{6+2+}$ | | – | – | 3.5 | – | – | – | | 5 | 7,10 | 6 | | | |
| Setup Time Data | $t_{setup}$ | 2 | – | – | 1.5 | – | – | – | ns | – | 6,7 | 4,10 | 2 | 8 | 1,16 |
| Select | $t_{setup}$ | 2 | – | – | 2.5 | – | – | – | ns | 6 | 7,11 | 6,10 | 2 | 8 | 1,16 |
| Hold Time Data | $t_{hold}$ | 2 | – | – | 0.0 | – | – | – | ns | – | 6,7 | 4,10 | 2 | 8 | 1,16 |
| Select | $t_{hold}$ | 2 | – | – | −0.5 | – | – | – | ns | 5 | 7,11 | 6,10 | 2 | 8 | 1,16 |
| Rise Time (20% to 80%) | $t_{2+}$ | 2 | – | – | 2.0 | – | – | – | ns | – | 6,7,10 | 4 | 2 | 8 | 1,16 |
| Fall Time (20% to 80%) | $t_{2-}$ | 2 | – | – | 2.0 | – | – | – | ns | – | 6,7,10 | 4 | 2 | 8 | 1,16 |

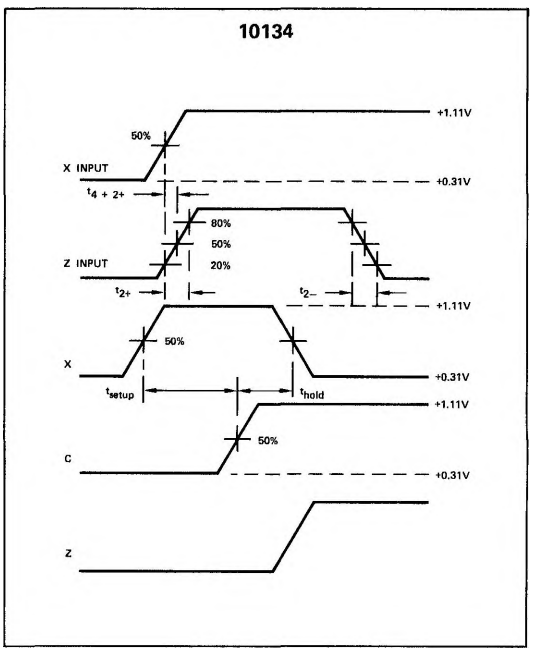
*All other inputs tested in the same manner

## SWITCHING TIME TEST CIRCUIT




INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

## PROPAGATION DELAY WAVEFORMS @ 25°C




NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from $TP_{in}$ to input pin and $TP_{out}$ to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.