

10113B, F: -30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

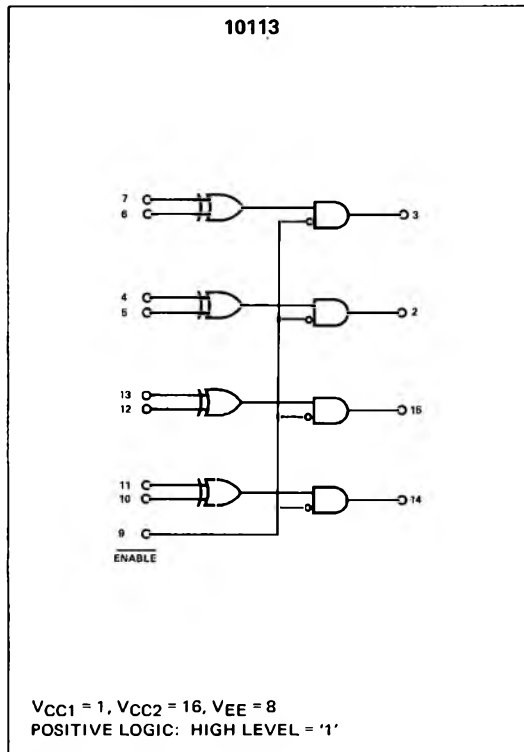
DESCRIPTION

The 10113 is a four gate array designed to provide the positive logic Exclusive OR function in high performance applications. This device contains a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over temperature. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE} .

Open emitter outputs are provided to enable bussing of multiple outputs together. If the four outputs of the 10113 are wire-ORed together the device performs a 4-bit compare function (outputs low for compare).

The outputs are all gated by the enable input. If this enable input is high all outputs will be forced low.

LOGIC DIAGRAM



FEATURES

- PERFORMS 4-BIT COMPARE FUNCTION (IF OUTPUTS ARE WIRE-ORed TOGETHER)
- HIGH FUNCTIONAL DENSITY – FOUR EXCLUSIVE OR GATES/PACKAGE
- FAST PROPAGATION DELAY FOR EXCLUSIVE OR: 2.5 ns TYP
- LOW POWER DISSIPATION: 165 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE FOUR 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: $V_{EE} = -5.2 V \pm 5\%$ RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- OUTPUT ENABLE GATING MAKES POWERFUL LOGIC FUNCTION

APPLICATIONS

- QUAD EXCLUSIVE-OR
(For parity, error correcting, and other logic functions).
- FOUR-BIT COMPARATOR
(For logic, test equipment, error detection applications).
- GATED FOUR-BIT COMPARATOR
(Enable input permits wire-ORing multiples of four bits)

TRUTH TABLE

$\overline{E9}$	IN 7	IN 6	OUT 3
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	ϕ	ϕ	L

ϕ = Don't Care.

TEMPERATURE RANGE

- -30 to +85°C Operating Ambient

PACKAGE TYPES

- B: 16-Pin Silicone DIP
- F: 16-Pin CERDIP

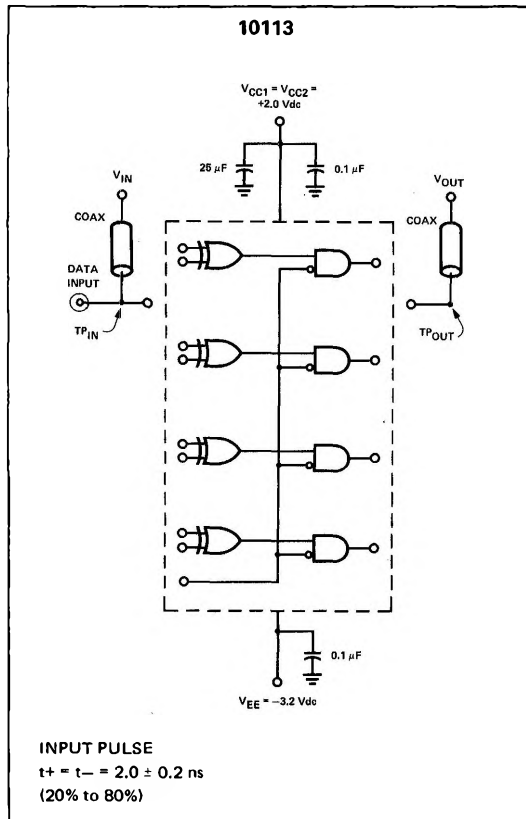
ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

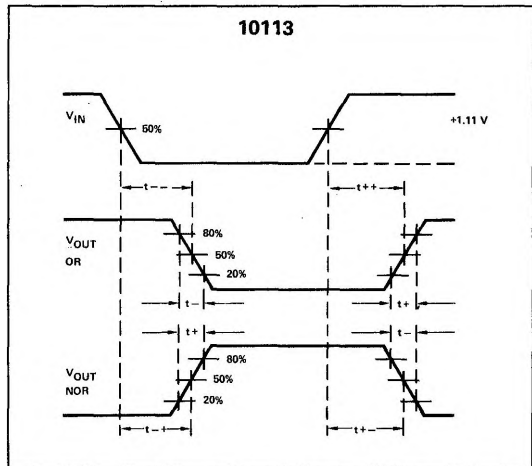
Characteristic	Symbol	Pin Under Test	10113 Test Limits						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Grd
			-30°C		+25°C		+85°C			V _{IH} max	V _{IL} min	V _{IHA} min	V _{ILA} max	V _{EE}	
			Min	Max	Min	Max	Min	Max							
Power Supply Drain Current	I _E	8	—	—	—	40	—	—	mAdc	—	—	—	—	8	1,16
Input Current	I _{inH}	6,7	—	—	—	265	—	—	μAdc	6,7	—	—	—	8	1,16
	I _{inL}	9	—	—	—	720	—	—	μAdc	9	—	—	—	8	1,16
	I _{inL}	*	—	—	0.5	—	—	—	μAdc	—	*	—	—	8	1,16
Logic "1" Output Voltage	V _{OH}	3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	6	—	—	—	8	1,16
	V _{dc}	3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7	—	—	—	8	1,16
Logic "0" Output Voltage	V _{OL}	3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	—	—	—	—	8	1,16
	V _{dc}	3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	6,7	—	—	—	8	1,16
Logic "1" Threshold Voltage	V _{OHA}	3	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	6	—	8	1,16
	V _{dc}	3	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	7	—	8	1,16
Logic "0" Threshold Voltage	V _{OLA}	3	—	-1.655	—	-1.570	—	-1.595	Vdc	7	—	6	—	8	1,16
	V _{dc}	3	—	-1.655	—	-1.630	—	-1.595	Vdc	—	—	6	—	8	1,16
Switching Times: [†] (50 Ω load) Propagation Delay	t _{PH}	3			Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t _{PL}	↓							ns	—	—	6	3	8	1,16
	t _{HL}	↓								7	—	—	—	—	—
	t _{HL}	↓								7	—	—	—	—	—
Rise Time (20% to 80%) Fall Time (20% to 80%)	t _r	2,3,14,15								4,7,11,13		9	2,3,14,15		
	t _r	↓								—		—	—	—	—
	t _f	↓								—		—	—	—	—
	t _f	↓								—		—	—	—	—

* Individually test each input applying V_{IH} or V_{IL} to input under test.
 ** Any Output
 † Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a linear printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
- For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.