100370

100370 Low Power Universal Demultiplexer/Decoder



Literature Number: SNOS126

100370 Low Power Universal Demultiplexer/Decoder

General Description

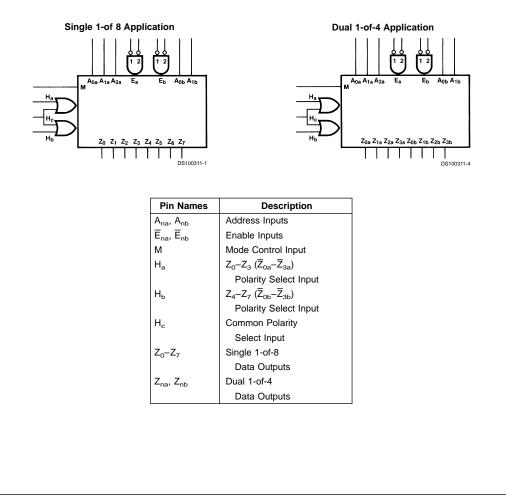
Logic Symbols

The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable (\bar{E}) inputs. Pin assignments for the \bar{E} inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables (\bar{E}_{1a} to \bar{E}_{2a} to \bar{E}_{2b}). Signals applied to auxiliary inputs H_a , H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a} , A_{1a} and A_{0b} ,

 A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 k Ω pulldown resistors.

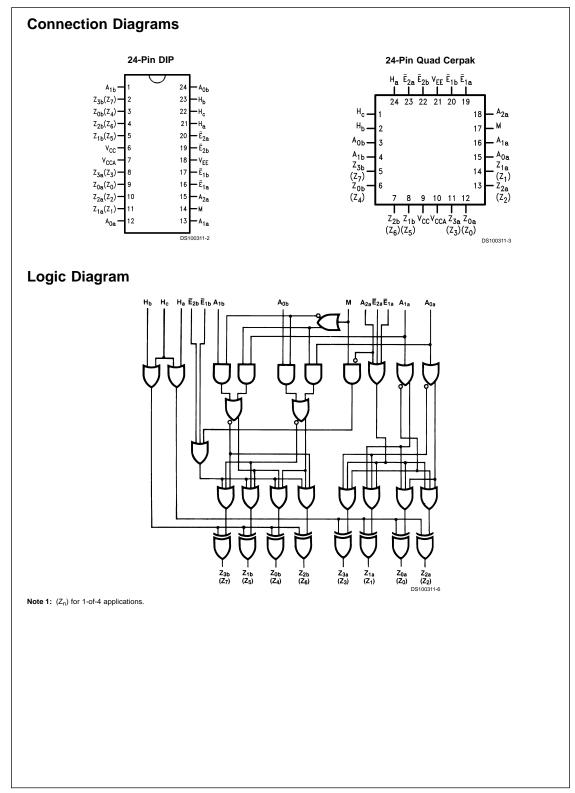
Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range = -4.2V to -5.7V



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Truth Tables

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)

Inputs				Active HIGH Outputs (H _a and H _b Inputs HIGH)				Active LOW Outputs (H _a and H _b Inputs LOW)			
Ē _{1a} Ē _{1b}	\overline{E}_{2a} \overline{E}_{2b}	A _{1a} A _{1b}	A _{0a} A _{0b}	Z _{0a} Z _{0b}	Z _{1a} Z _{1b}	Z _{2a} Z _{2b}	Z _{3a} Z _{3b}	Z _{0a} Z _{0b}	Z _{1a} Z _{1b}	Z _{2a} Z _{2b}	Z _{3a} Z _{3b}
Н	Х	Х	Х	L	L	L	L	Н	Н	Н	Н
Х	н	Х	Х	L	L	L	L	н	Н	н	н
L	L	L	L	Н	L	L	L	L	Н	Н	н
L	L	L	н	L	н	L	L	н	L	н	н
L	L	н	L	L	L	н	L	н	н	L	н
L	L	н	н	L	L	L	н	н	н	н	L

Single 1-of-8 Mode (M = HIGH; $A_{0b} = A_{1b} = H_a = H_b = LOW$)

Inputs						Active HIGH Outputs (Note 2) (H _c Input HIGH)							
Ē1	Ē ₂	A _{2a}	A _{1a}	A_{0a}	Zo	Z ₁	Z ₂	Z ₃	Z_4	Z ₅	Z ₆	Z 7	
н	Х	Х	Х	Х	L	L	L	L	L	L	L	L	
X	н	х	x	х	L	L	L	L	L	L	L	L	
L	L	L	L	L	н	L	L	L	L	L	L	L	
L	L	L	L	н	L	н	L	L	L	L	L	L	
L	L	L	н	L	L	L	н	L	L	L	L	L	
L	L	L	н	н	L	L	L	н	L	L	L	L	
L	L	н	L	L	L	L	L	L	Н	L	L	L	
L	L	н	L	н	L	L	L	L	L	н	L	L	
L	L	н	н	L	L	L	L	L	L	L	н	L	
L	L	н	н	н	L	L	L	L	L	L	L	Н	

H = HIGH Voltage Level L = LOW Voltage Level

 $\begin{array}{l} X = \text{Don't Care} \\ \overline{E}_1 = \overline{E}_{1a} \text{ and } \overline{E}_{1b} \text{ wired}; \ \overline{E}_2 = \overline{E}_{2a} \text{ and } \overline{E}_{2b} \text{ wired} \end{array}$

Note 2: for H_c = LOW, output states are complemented

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired.

–65°C to +150°C
+175°C
-7.0V to +0.5V
V _{EE} to +0.5V
–50 mA

Military Version DC Electrical Characteristics

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$V_{EE} = -4.2V$ to -5.7V, $V_{CC} = V_{CCA} = GND$, $T_{C} = -55^{\circ}C$ to +125°C

ESD (Note 4)

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Tc	Conditions		Notes
		-1025	-870	mV	0°C to			
V _{он}	Output HIGH Voltage				+125°C			
		-1085	-870	mV	–55°C	V _{IN} = V _{IH} (Max)	Loading with	(Notes 5, 6, 7)
		-1830	-1620	mV	0°C to	or V _{IL} (Min)	50Ω to -2.0V	
V _{OL}	Output LOW Voltage				+125°C			
		-1830	-1555	mV	–55°C			
		-1035		mV	0°C to			
V _{OHC}	Output HIGH Voltage				+125°C			
		-1085		mV	–55°C	$V_{IN} = V_{IH}$ (Min)	Loading with	(Notes 5, 6, 7)
			-1610	mV	0°C to	or V _{IL} (Max)	50Ω to -2.0V	
V _{OLC}	Output LOW Voltage				+125°C			
			-1555	mV	–55°C			
VIH	Input HIGH Voltage	-1165	-870	mV	–55°C to	Guaranteed HIGH Signal for All Inputs		(Notes 5, 6, 7, 8)
					+125°C			
VIL	Input LOW Voltage	-1830	-1475	mV	–55°C to	Guaranteed LOW Signal for		(Notes 5, 6, 7, 8)
					+125°C	All Inputs		
I _{IL}	Input LOW Current	0.50		μA	–55°C to	$V_{EE} = -4.2V$		(Notes 5, 6, 7)
					+125°C	$V_{IN} = V_{IL}$ (Min)		
IIH	Input HIGH Current							
			240	μA	25°C to			
					+125°C			
						$V_{EE} = -5.7V$		(Notes 5, 6, 7)
			340	μA	–55°C	$V_{IN} = V_{IH}$ (Max)		
I_{EE}	Power Supply Current	-105	-36	mA	–55°C to	Inputs Open		(Notes 5, 6, 7)
					+125°C			

Note 5: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C, then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 6: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 7: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 8: Guaranteed by applying specific input condition and testing V_{OH}/V_{OL} .

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≥2000V

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND											
Symbol	Parameter	T _c = -55°C		T _C = +25°C		T _c = +125°C		Units	Conditions	Notes	
		Min	Max	Min	Max	Min	Max				
t _{PLH}	Propagation Delay	0.3	2.40	0.4	2.20	0.40	2.70	ns			
t _{PHL}	\overline{E}_{na} , \overline{E}_{nb} to Output										
t _{PLH}	Propagation Delay	0.30	2.60	0.40	2.40	0.40	2.90	ns			
t _{PHL}	A _{na} , A _{nb} to Output									(Notes 9, 10,	
t _{PLH}	Propagation Delay	0.30	2.60	0.40	2.40	0.40	2.40	ns	Figures 1, 2	11)	
t _{PHL}	H_a , H_b , H_c to Output										
t _{PLH}	Propagation Delay	0.40	3.10	0.60	2.80	0.70	3.70	ns			
t _{PHL}	M to Output										
t _{TLH}	Transition Time	0.30	1.60	0.30	1.60	0.30	1.60	ns		(Note 12)	
t _{THL}	20% to 80%, 80% to 20%										

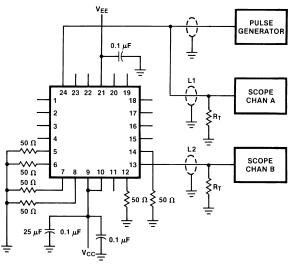
Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 11: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and -55°C Temp., Subgroups A10 and A11.

Note 12: Not tested at +25°C, +125°C and -55°C Temperature (design characterization data).

Test Circuit

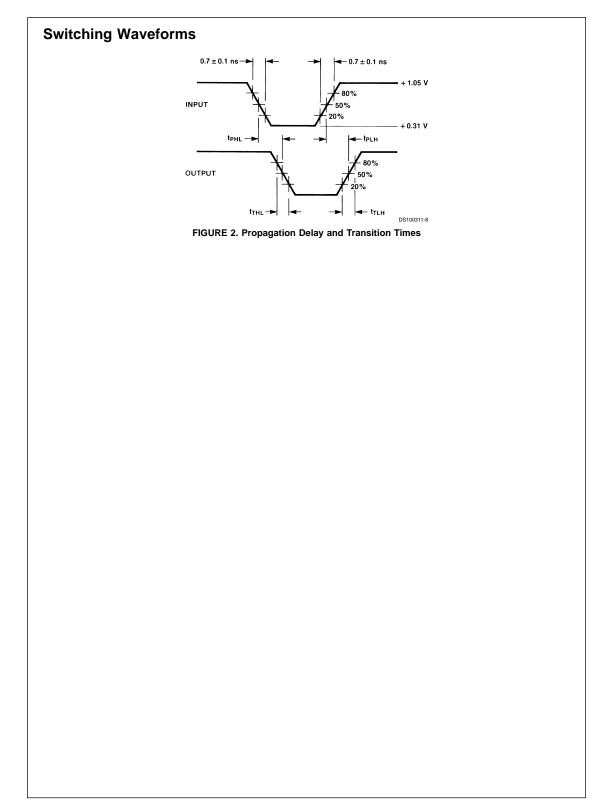


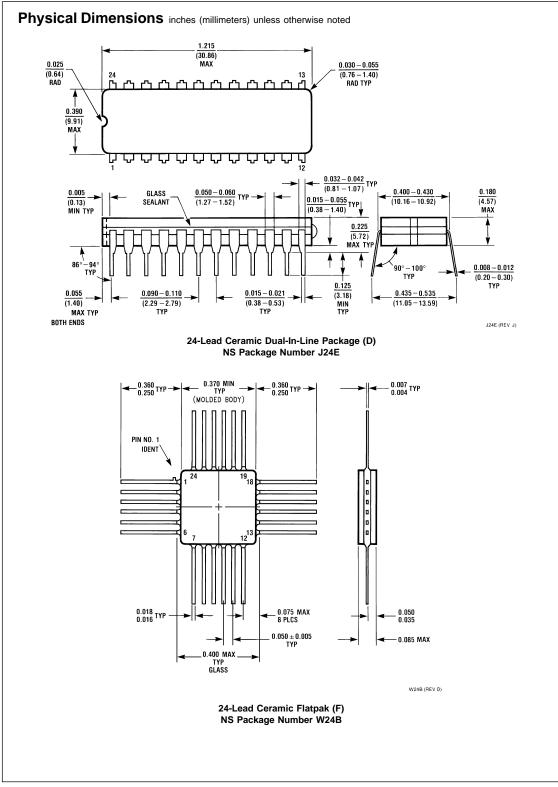
DS100311-7

Notes:

 $\begin{array}{l} \text{NOLS.}\\ \text{V}_{CC}, \text{V}_{CCA} = +2\text{V}, \text{V}_{EE} = -2.5\text{V}\\ \text{L1 and L2} = \text{equal length } 50\Omega \text{ impedance lines}\\ \text{R}_{T} = 50\Omega \text{ terminator internal to scope}\\ \text{Decoupling 0.1 } \mu\text{F from GND to } \text{V}_{CC} \text{ and } \text{V}_{EE}\\ \text{All unused outputs are loaded with } 50\Omega \text{ to GND}\\ \text{C}_{L} = \text{Fixture and stray capacitance} \leq 3 \text{ pF}\\ \text{Pin numbers shown are for flatpak; for DIP see logic symbol} \end{array}$

FIGURE 1. AC Test Circuit





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