100370

100370 Low Power Universal Demultiplexer/Decoder

Literature Number: SNOS126

National Semiconductor

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100370
Low Power Universal Demultiplexer/Decoder

General Description

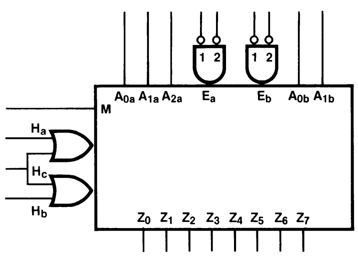
The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ($\overline{E}_{1a}$ to $\overline{E}_{1b}$, $\overline{E}_{2a}$ to $\overline{E}_{2b}$). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 kΩ pulldown resistors.

Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range = −4.2V to −5.7V

Logic Symbols

Single 1-of 8 Application



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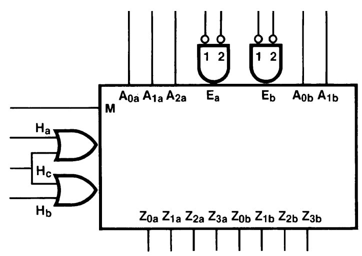
Dual 1-of-4 Application



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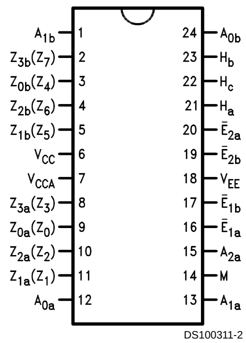
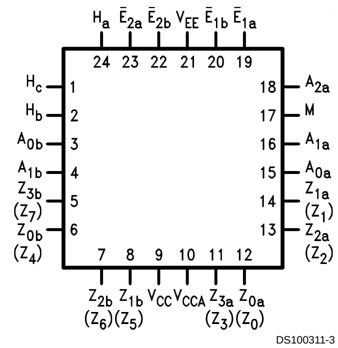
Pin Names	Description
A_{na}, A_{nb}	Address Inputs
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs
M	Mode Control Input
H_a	Z_0–Z_3 ($\overline{Z}_{0a}$–$\overline{Z}_{3a}$) Polarity Select Input
H_b	Z_4–Z_7 ($\overline{Z}_{0b}$–$\overline{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
Z_0–Z_7	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs

Connection Diagrams

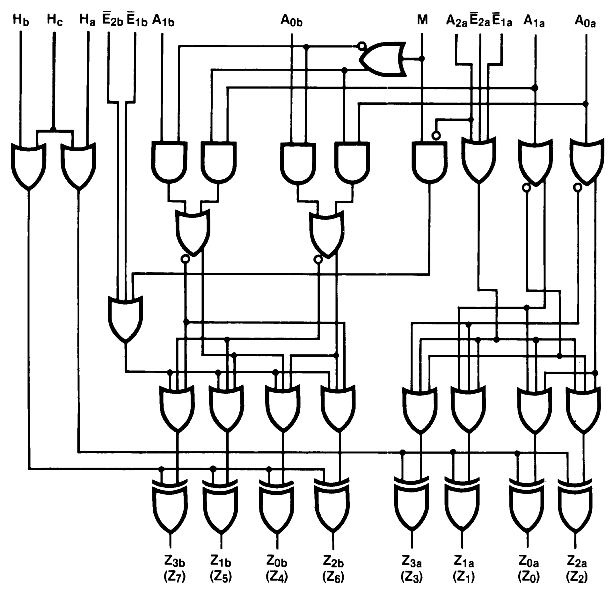
24-Pin DIP



24-Pin Quad Cerpak



Logic Diagram



Note 1: (Z_n) for 1-of-4 applications.

Truth Tables

Dual 1-of-4 Mode ($M = A_{2a} = H_c$ = LOW)

Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; $A_{0b} = A_{1b} = H_a = H_b$ = LOW)

Inputs					Active HIGH Outputs (Note 2) (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
$\overline{E}_1 = \overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2 = \overline{E}2_{2a}$ and $\overline{E}_{2b}$ wired

Note 2: for H_c = LOW, output states are complemented

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 4)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 3: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 5, 6, 7)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	(Notes 5, 6, 7)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs		(Notes 5, 6, 7, 8)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs		(Notes 5, 6, 7, 8)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 5, 6, 7)
I_{IH}	Input HIGH Current		240	µA	25˚C to +125˚C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(Notes 5, 6, 7)
			340	µA	−55˚C			
I_{EE}	Power Supply Current	−105	−36	mA	−55˚C to +125˚C	Inputs Open		(Notes 5, 6, 7)

Note 5: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C, then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 6: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 7: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 8: Guaranteed by applying specific input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.3	2.40	0.4	2.20	0.40	2.70	ns	*Figures 1, 2*	(Notes 9, 10, 11)
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.30	2.60	0.40	2.40	0.40	2.90	ns		
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.30	2.60	0.40	2.40	0.40	2.40	ns		
t_{PLH} t_{PHL}	Propagation Delay M to Output	0.40	3.10	0.60	2.80	0.70	3.70	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.60	0.30	1.60	0.30	1.60	ns		(Note 12)

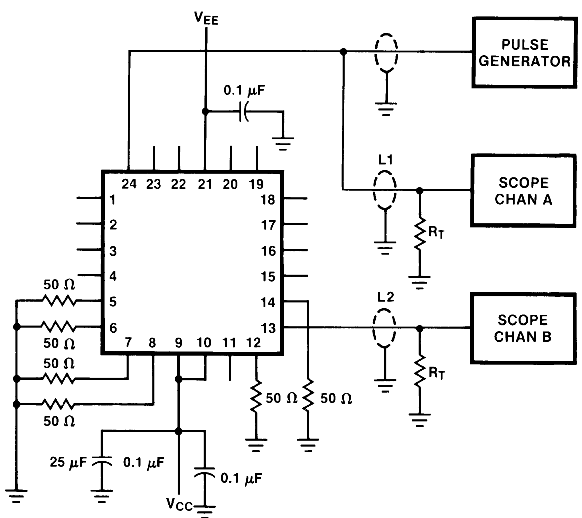
Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at +25˚C, temperature only, Subgroup A9.

Note 11: Sample tested (Method 5005, Table I) on each Mfg. lot at +25˚C, Subgroup A9, and at +125˚C, and −55˚C Temp., Subgroups A10 and A11.

Note 12: Not tested at +25˚C, +125˚C and −55˚C Temperature (design characterization data).

Test Circuit



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Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Switching Waveforms

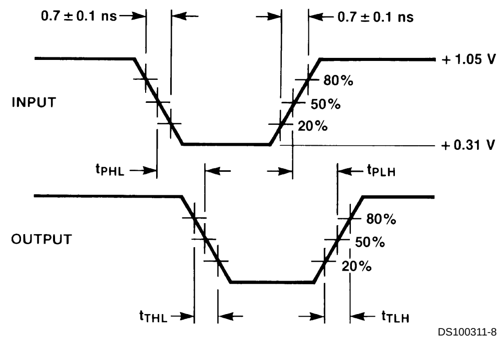
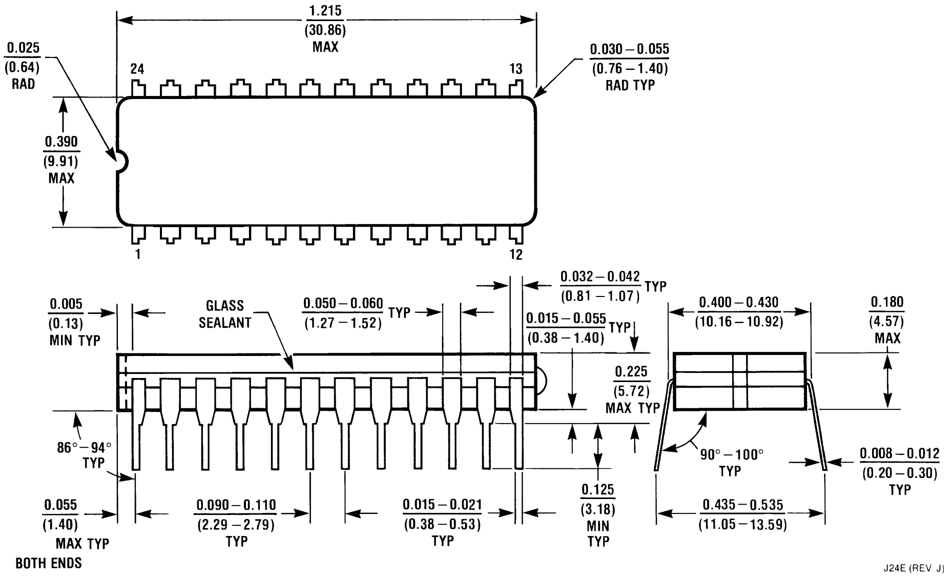
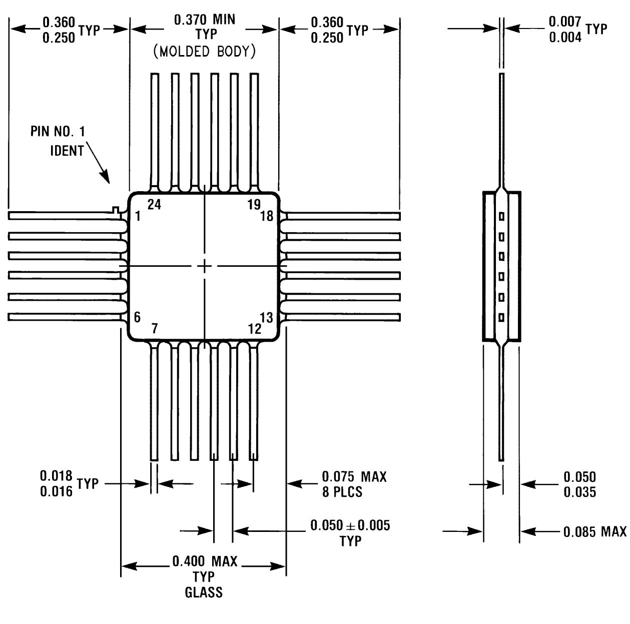


FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Lead Ceramic Flatpak (F)
NS Package Number W24B

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179